॥जय गुरुजी॥ ॥जय गुरुराम॥

SUB:- DTE (313303)

Prepared By :-

Unit 2 :- Logic Gates and Boolean Algebra.

Prof. Swapnil J. Bafana

⊛ Logic families :-

i) Def^{n} :- Logic families are defined as → the type of logic circuit → or group of logic circuits → used in an IC [Integrated Circuit]

ii) Common logic families are →

a) TTL [Transistor Transistor Logic]

b) CMOS [Complementary Metal Oxide Semiconductor].

c) RTL [Registor Transistor Logic]

d) ECL [Emitter Coupled Logic]

e) DTL [Diode Transistor Logic]

⊛ Characteristics parameters of Digital Logic families :-

A) **Noise Margin** :- A Quantitative Measures of Noise Immunity of a Logic family → is called "Noise Margine".

A.1) **Noise Immunity** :- An ability of logic Circuit → to tolerate the noise → without changing its output is Called "Noise Immunity".

A.2) **Noise** :- It is an Unwanted signal or unwanted disturbance which can change the output.

B) **Power Dissipation** :- It is defined as → the amount of power Consumed and Converted in the form of Heat.

C) **Figure of Merit (Speed power Product)** :- It is defined as → the product of → power dissipation and propogation Delay.

∴ Figure of Merit = power Dissipation * propogation Delay

D) **Propogation Delay (Speed of operation)** :- The output of a logic gate → does not change it's state instantaneously → when the state of it's input is changed.

E) **Fan IN** :- It is defined as → the number of inputs a gate has.
e.g. for Two inupt gate → fanin = 02

F) **fan out** :- It is defined as → the maximum number of inputs → that an output of the gate → Can drive without falling outside the specified output voltage.
e.g. fan out = 5 → indicates that the gate Can drive → at the most 5 inputs of same Ic family.

G) **Maximum clock frequency** :- It is the Highest frequency → of Square wave signal → that the logic gates Can process without errors.

H) **Supply Voltage Requirement** :- It is minimum and maximum voltages required for proper operation of the logic family.

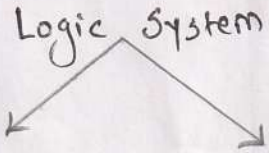
I) **Power per Gate** :- It indicates that the Average power Consumption per logic gate within logic family.

✱ **Compare TTL, CMOS and ECL** :- (Sir says Do Not Pay for AUG Competetion)

Parameter	TTL	CMOS	ECL
1) Stands for	Transistor Transistor Logic	Complementary Metal oxide Semiconductor	Emitter Coupled Logic
2) Speed power product	100 pJ	0.7 pJ	50-100 pJ
3) Delay	10 ns	70 ns	2 ns
4) Noise Margine	Moderate	High	low
5) Power Dissipation	10 mW (milli watt)	0.1 mW (milli watt)	40-50 mW (milliWatt)

Parameter	TTL	CMOS	ECL
6) Fan out	Moderate (10)	Highest (50)	High. (25)
7) Application	Lab & portable equipment, (High speed switching Application.)	Portable Equipment	High speed Switch application
8) Used Components	Transistor, Diodes & Resistors	MOSFET's	Resistors & Transistors.
9) Gates	NAND	NAND/NOR	OR/NOR
10) Complexity	Complex	Moderately Complex	Complex

✱ **Logic Systems :-** Logic system defines → about voltage level Corresponds to Binary values → usually 0 & 1.



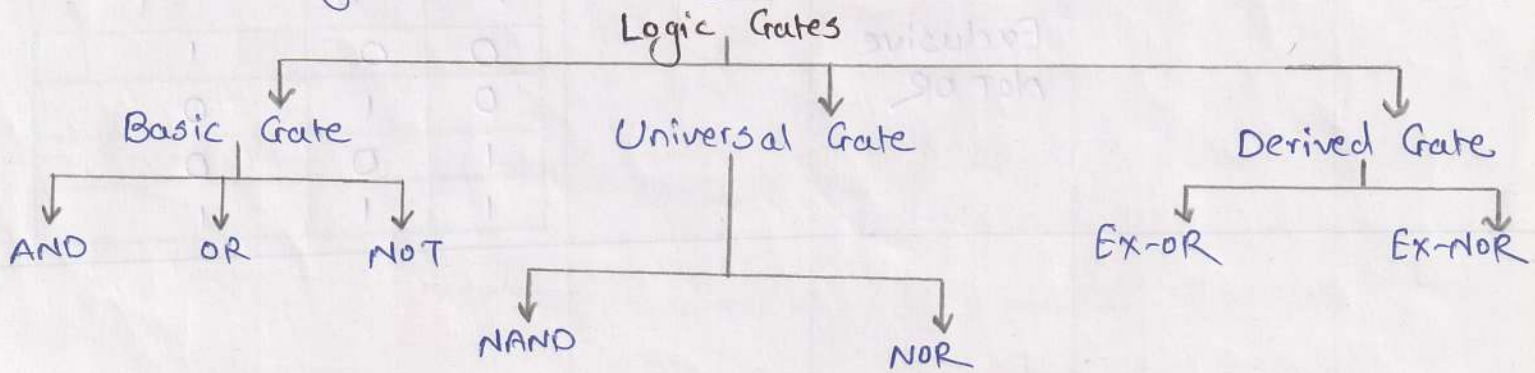
Positive Logic System

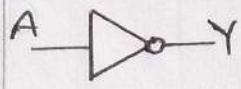
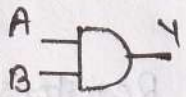
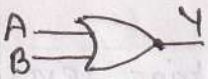
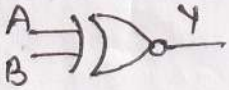
1) Higher voltage level → represents → Logic 1
2) Lower voltage level → represents → logic 0

Negative Logic System

1) Higher voltage level → represents Logic 0.
2) Lower voltage level → represents Logic 1.

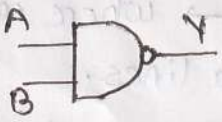
✱ **Logic Gates :-** Logic Gates are logic circuits → which acts as a Basic Building Blocks of any Digital system.



Gate	Symbol	Expression & operation	Ic No.	Truth Table
1) NOT Gate or Inverter		$Y = \overline{A}$ (Inversion)	IC 7404	Input: A; Output: Y 0 → 0 → 1 1 → 1 → 0
2) AND Gate		$Y = AB$ (Multiplication)	IC 7408	Input: A, B; Output: Y 0 0 0 0 1 0 1 0 0 1 1 1
3) OR Gate		$Y = A + B$ (Addition)	IC 7432	Input: A, B; Output: Y 0 0 0 0 1 1 1 0 1 1 1 1
4) Ex-OR Gate		$Y = A \oplus B$ Exclusive OR	IC 7486	Input: A, B; Output: Y 0 0 0 0 1 1 1 0 1 1 1 0
5) Ex-NOR Gate		$Y = \overline{A \oplus B}$ Exclusive NOT OR	IC 74266	Input: A, B; Output: Y 0 0 1 0 1 0 1 0 0 1 1 1

Gate	Symbol	Expression & operation	IC No.	Truth Table

6) NAND Gate



$Y = \overline{AB}$

IC 7400

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

7) NOR Gate

$Y = \overline{A+B}$

IC 7402

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

✱ **Buffer** :- i) It is a digital logic circuit → that passes signal → from i/p to o/p → without changing it's logic level → but with increased Driving Capability.

ii) Buffers are used → when signal needs to travel long distance or drive multiple inputs.

iii) **Purpose of Buffer** :- a) Signal Amplification
b) Isolation between input & output
c) Prevent loading effects.
d) Control data flow in systems with shared Buses.

iv) It does not perform any logic operation → like AND, OR etc

v) In Digital system → buffers are used → to control → signal flow, → improve signal integrity and manage timing.

vi) **Types of Buffer** :- A) Tri-state Buffer
B) Bidirectional Buffer
C) Unidirectional Buffer
D) Inverting Buffer
E) Non-inverting Buffer

✱ **Tri-state logic** :- i) It is a type of digital logic → where a signal can exist → in 3 different output states.

ii) 3 different output states are → a) High (1)
b) low (0)
c) High Impedance (Hi-Z)

iii) Purpose of Tristate logic :-

a) Used in Bus system and Memory system → where many devices may need to send data → over the same data lines.

b) It prevents conflicts by ensuring → only one device drives the line at a time.

c) It allows a device → to disconnect from → the Bus using Hi-Z state → so another device can send data without interference.

iv) It Enables Bus sharing → without short circuits.

v) Reduces pincount in circuits → by allowing multiple devices to use same lines.

vi) It improves modularity in digital systems.

Enable (E)	Input A	output Y
1	0	0
1	1	1
0	X	Hi-Z

* Compare Unidirectional and Bidirectional :-

Parameters	Unidirectional Buffer	Bidirectional Buffer.
1) Data Flow Direction	one way only (input → output)	Two way (input ⟷ output)
2) Number of Buffers needed	one per Direction	Two → (one for each dir^n)
3) Control Signals	Enable (E)	Enable (E) + Direction Control (DIR)
4) Complexity	Simple	More Complex
5) Typical Use Case	Driving a data line or isolating a signal	Shared Communication line
6) Bus Compatibility	Suitable for writing or reading only	Suitable for both → reading from & writing to a bus
7) Tri-State Compatibility	YES	YES.

Parameters	Unidirectional Buffer			Bidirectional Buffer.		
8) operation	Input (A)	Enable (E)	output (Y)	Direction	Enable	function
	0	1	0	0	1	B→A (read)
	1	1	1	1	1	A→B (write)
	X	0	Hi-Z	X	0	Hi-Z (No flow)

⊛ Boolean Algebra :- i) It is used to Analyze and simplify → the digital circuits.

ii) It uses only the Binary numbers i.e. of 1.
Hence it is also called as → "Binary Algebra" or "Logical Algebra".

iii) Rules in Boolean laws :-

a) Variables used → Can have only two values →
e.g. Binary 1 → for High
Binary 0 → for low

b) Complement of a Variable → is represented by → overbar (−).
e.g. if $B=0$ then $\overline{B}=1$
$B=1$ then $\overline{B}=0$

c) ORing of Variables → is represented by → plus (+) sign between them.
e.g. ORing of A, B, C is represented as $A+B+C$.

d) Logical ANDing of two or more Variables is represented by writing a dot between them such as $A \cdot B \cdot C \cdot D \cdot E \cdot F$.

⊛ Boolean Laws :-

1) Commutative Law :- It states that → we can change the sequence of input → without having any effect on output.

e.g. $A + B = B + A$

A	B	A+B	B+A
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

$A \cdot B = B \cdot A$

A	B	A·B	B·A
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

2) Associative law :- It states that → the order in which → logic operations are performed → is not at all important → as ultimate outcome is the same.

e.g. $(A \cdot B) \cdot C = A \cdot (B \cdot C)$

			LHS		RHS
A	B	C	A·B	(A·B)·C	A·(B·C)
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	1	1

$(A+B)+C = A+(B+C)$

			LHS	RHS
A	B	C	(A+B)+C	A+(B+C)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

3) Distributive law :- It states that → Product of an input with sum of two other inputs → is equals to → the sum of product of first two inputs and product of first and last input.

e.g. $A \cdot (B+C) = AB + AC$

				LHS			RHS
A	B	C	(B+C)	A·(B+C)	AB	AC	AB+AC
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

4) AND law :- i) It is related to AND operation → hence called as "AND law".

ii) AND laws are as follows

1) $A \cdot 0 = 0$
2) $A \cdot 1 = A$
3) $A \cdot A = A$
4) $A \cdot \overline{A} = 0$

5) OR law :- i) It is related to OR operation → hence called as "OR law".

ii) OR laws are as follows

1) $A + 0 = A$
2) $A + 1 = 1$
3) $A + A = A$
4) $A + \overline{A} = 1$

6) Inversion law :- It states that → if a variable is subject to double Inversion, then it will be result in the original value itself.

A	$\overline{A}$	$\overline{\overline{A}}$
0	1	0
1	0	1

✱ Duality Theorem :- i) It states that → the dual of an Algebric expression → can be obtained simply by → interchanging OR and AND operators and by replacing 1s by 0s and 0s by 1s.

ii) According to Duality Theorem, following Conversion is possible in given Boolean expression

a) Change each AND operation to OR operation.
b) Change each OR operation to AND operation.
c) Complement any 1 or 0 appearing in the expression.

iv) e.g. Dual of $A(B+C) = AB+AC$ is given below,

$$A+(B\cdot C) = (A+B)\cdot(A+C)$$

⊛ Demorgan's Theorem :-

A) Demorgan's 1st theorem :-

i) Eqⁿ is, $\boxed{\overline{A+B} = \overline{A}\cdot\overline{B}}$

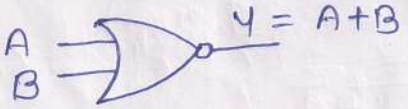
ii) It states that → the Complement of Addition of Two inputs is equal to Product of their individual Complement.

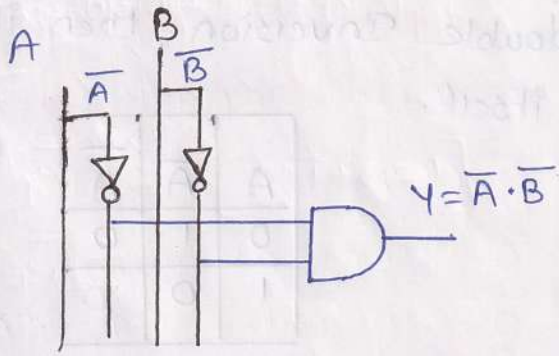
iii)

		LHS				RHS
A	B	A+B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

LHS = RHS

iv)



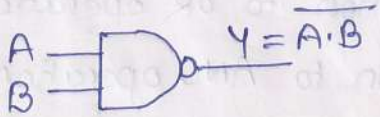


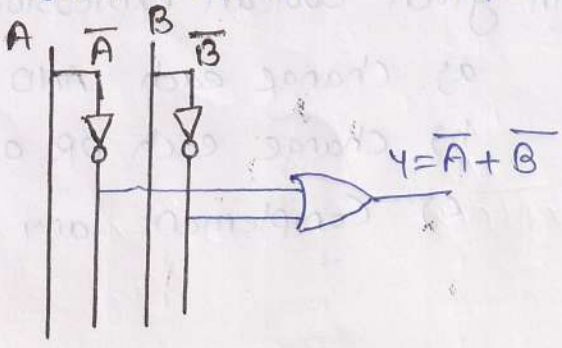
B) Demorgan's 2nd Theorem :-

i) Eqⁿ is $\boxed{\overline{A\cdot B} = \overline{A}+\overline{B}}$

ii) It states that → Complement of Product of Two inputs is equals to addition of their individual Complement.

iii)





iv)

A	B	A·B	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$	
0	0	0	1	1	1	1	Here, LHS = RHS Hence, it is proved.
0	1	0	1	1	0	1	
1	0	0	1	0	1	1	
1	1	1	0	0	0	0	

Q.1 Reduce the following Expression and implement it using logic gates

i) $Y = (\overline{AB} + \overline{A+B})\, A \cdot \overline{B}$

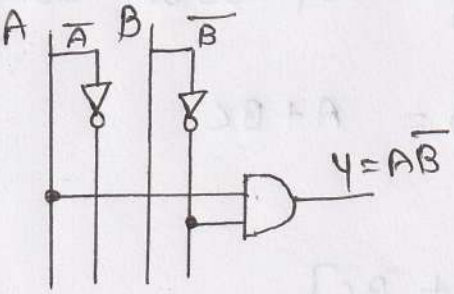
$= (\overline{A} + \overline{B} + \overline{A} \cdot \overline{B})\, A \cdot \overline{B}$ ---(Demorgan's 1st & 2nd) Thm.

$= \overline{A} \cdot A \cdot \overline{B} + \overline{B} \cdot A \cdot \overline{B} + A\overline{A} \cdot \overline{B} \cdot \overline{B}$

$= 0 + A\overline{B} + 0$ --- $[A \cdot \overline{A} = 0]$

$Y = A\overline{B}$ --- $[\overline{B} \cdot \overline{B} = \overline{B}]$

Logic Dia:-



ii) Implement the logical expression using logic Gates.

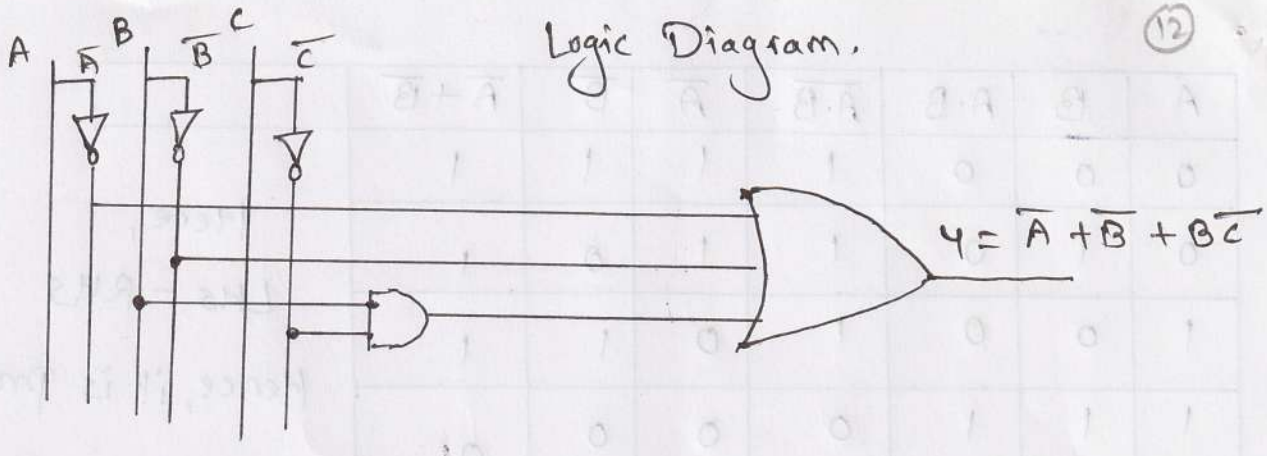
$Y = \overline{AB} + \overline{A}C + B\overline{C}$

$= \overline{A} + \overline{B} + \overline{A}C + B\overline{C}$

$= \overline{A}[1+C] + \overline{B} + B\overline{C}$

$\therefore Y = \overline{A} + \overline{B} + B\overline{C}$ --- $[\because 1+C=1]$

Logic Diagram.



iii) Simplify the following Boolean expression & implement it using logic gates

$$Y = AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$$

$\Rightarrow$

$$Y = AB\bar{C}[\bar{D}+D] + ABC[\bar{D}+D]$$

$$= [\bar{D}+D]\,AB\bar{C} + [\bar{D}+D]\,ABC$$

$$= AB\bar{C} + ABC \quad \text{--- } [\bar{D}+D=1]$$

$$= AB[\bar{C}+C]$$

$$Y = AB \quad \text{--- } [\bar{C}+C=1]$$

iv) Prove the following logic expression using Boolean Algebra.

$$(A+B)(A+C) = A+BC$$

$\Rightarrow$

$$LHS = (A+B)(A+C)$$

$$= [A\cdot A + A\cdot C + AB + BC]$$

$$= A + AC + AB + BC \quad \text{--- } [A\cdot A = A]$$

$$= A[1+C] + B(A+C) \quad \text{--- } [1+C=1]$$

$$= A + AB + BC$$

$$= A[1+B] + BC \quad \text{--- } [1+B=1]$$

$$= A+BC$$

$$= RHS$$

S2 Bafana 29/05/2026

Mr. S. S. Bafana

29/5/26.

DIGITAL TECHNIQUES [DTE-313303]

Branch: CO / CW | **QUESTION BANK** | Year: - Second (2nd)

Semester: - Third (3rd) | **Unit 2: Logic Gates and Boolean Algebra** | Marks: 12 Marks

Q.1 02 Marks Question

i) Draw the following logic gates using "NAND" gates. ...(W-25)
   a) AND gate b) NOR gate

ii) Draw the symbol & write truth table of NAND gate. ...(S-25)

iii) State the difference in logic of EX-OR and EX-NOR gate ...(S-25)

iv) List OR laws of Boolean Algebra ...(W-24)

v) Simplify following expression with Boolean laws, ...(W-24)
   $Y = (A+B)(A+C)$

vi) Define i) Noise Margine ii) figure of merit ...(W-24)

vii) Define i) power dissipation ii) speed of operation.

viii) Define i) fan in ii) fan out

ix) Draw the Symbol & Truth Table of AND gate & OR gate

x) Draw the Symbol & Truth Table of NOT gate & NOR gate

xi) Compare Uni Directional & Bi-directional Buffer

Sr Bafana 29/05/2026

29/5/26

Q.2) 04 Marks Questions

i) State Demorgan's Theorems and write logical expression for both. or State & prove Demorgan's Theorem. → (W-25)

ii) State Concepts of following with proper diagram and give two examples of each → (W-25)

   i) Buffer
   ii) Tristate

iii) Simplify given expression, using Boolean laws and draw logic circuit for final expression → (W-25)

   i) $f = A\bar{B}C\bar{D} + ABC\bar{D} + A\bar{B}CD + ABCD + A\bar{B}\bar{C}D + AB\bar{C}D + AB\bar{C}\bar{D}$

iv) Implement following logic gates using "ONLY - NOR" realization write expression at different stages → (W-25)

   i) OR gate ii) NAND gate

v) State Duality Theorem. prove that AND laws and OR laws are dual of each other. → (S-25)

vi) Realize the logic operations of AND, OR, NOT gates using only NAND gates. → (S-25)

vii) Realize the following equations using NAND gate only. → (W-24)

   i) $Y = AB + CD$

   $Y = A + B$

viii) Compare TTL, CMOS and ECL (Any 4 points)

Bafana 29/05/2026

29/5/26