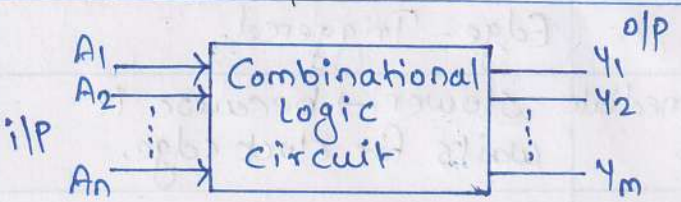
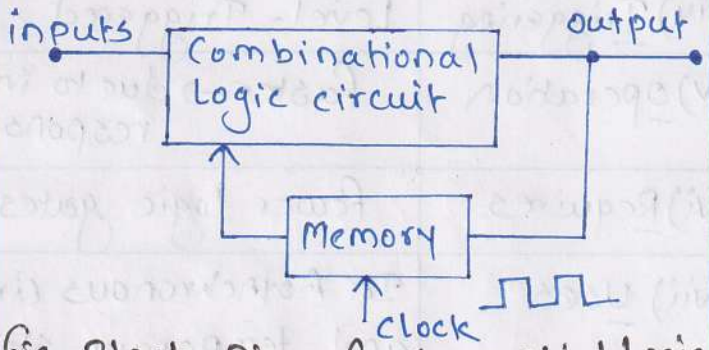
⊛ Difference between Combinational & Sequential Logic circuit

Combinational Logic circuit	Sequential Logic circuit
i) Def^ :- It is a digital ckt → in which → the output depends on → present inputs only.	i) Def^ :- It is a digital ckt → in which → the output depends on → present input and previous state → stored in memory elements.
ii) E.g. → Adder, Subtractor, multiplexer, Decoder etc.	ii) e.g. → Flipflop, Register, Counter etc.
iii) Can not store Data	iii) Can store Data
iv) Memory elements are not used.	iv) Memory elements are used.
v) Feedback path is Absent.	v) Feedback path is present.
vi) Clock signal is not required.	vi) Clock signal is required.
vii) Design & implementations are simple	vii) Design & implementations are more Complex.
viii) Faster operation → due to No memory.	viii) Slower operation → due to Memory & clocking.
 fig. Block Dia. of Combinational logic circuit.	 fig. Block Dia. of Sequential logic circuit.

⊛ Time independent (un-clocked) Logic system :-

i) Def^ :- It is a digital circuit → whose output depends only on the present inputs and does not require a clock signal for its operation.

ii) e.g. Latch, Adders, Multiplexer etc.

✱ Time dependent (clocked) logic system :-

i) Defⁿ :- It is a digital circuit → whose output depends on present inputs and past states and it operates under the control of clock signal.

ii) e.g. :- Flip-flop, Counters, Flip-flops, registers etc.

✱ Compare Latch and flip flop :-

Parameters	Latch	Flip-flop
i) Defⁿ :-	It is level-sensitive Bi-Stable storage Device that Can store one bit of Data and changes it's output whenever the enable or Control signal is Active.	It is an Edge-triggered Bistable storage Device that can store one bit of data and changes it's output only at specific Transition of clock signal.
ii) operates	Based on Enable signal.	Based on clock signal.
iii) Complexity	Simple circuit	More Complex circuit
iv) Triggering	Level-Triggered	Edge-Triggered.
v) operation	faster → due to immediate response	slower → because it waits for clock edge
vi) Requires	fewer logic gates	More logic gates.
vii) Uses	In Asynchronous circuits, and temporary storage	In synchronous circuits, registers, Counters etc
viii) Susceptible	More susceptible to unwanted changes and glitches	less susceptible to glitches and unwanted changes.

✱ Basic Memory Cell or 1-Bit Memory Cell :- flip flop is also known as Basic Digital Memory Circuit.

ii) Basic Memory cell → is the smallest unit of Memory → that Can store → one Binary Digit either 0 or 1.

iii) It has two stable states → Logic 1 state
→ Logic 0 state

iv) from the fig. → o/p of gate 1 is Connected to → i/p of gate 2 And o/p of gate 2 is Connected to i/p of gate 1.

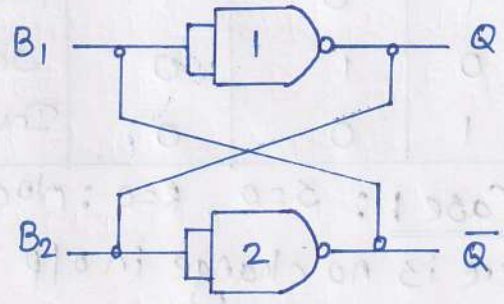


Fig. Cross Coupled Inverter as Memory Element.

v) if Q=0 then $\bar{Q}=1$ or
if Q=1 then $\bar{Q}=0$
o/p of circuit → will always be Complementary.

vi) Logic 1 state → Set state → $Q=1$ & $\bar{Q}=0$
Logic 0 state → Reset state → $Q=0$ & $\bar{Q}=1$

⊛ R-S latch using NOR gate

i) Logic Diagram :-

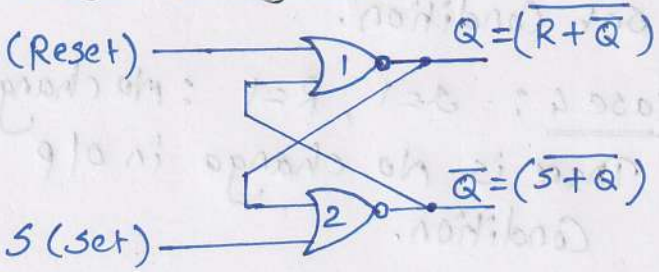


Fig. R-S latch using NOR gate.

ii) Symbol :-

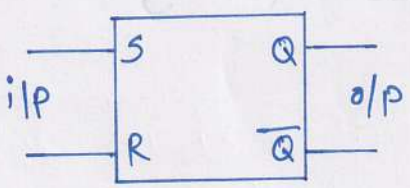


Fig. Symbol for S-R latch

⊛ R-S latch using NAND Gate

i) Logic Diagram :-

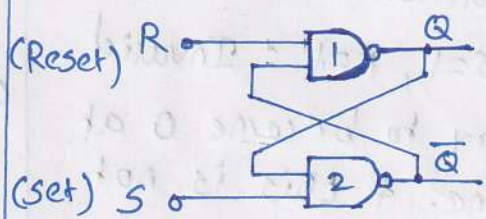


Fig. R-S latch using NAND gate

ii) Symbol :-

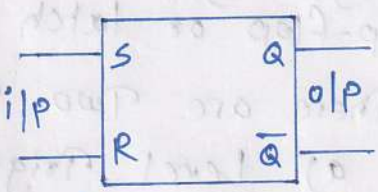


Fig. Symbol for S-R latch

R-S latch using NOR Gate

iii) Truth Table :-

S	R	Q	$\bar{Q}$	Remark
0	0	No change	No change	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Invalid

iv) Case 1 : S=0 , R=0 : No change
There is no change in o/p Condition.

Case 2 : S=0, R=1 : Reset
o/p Q=0 & $\bar{Q}$=1 & this is Reset Condition.

Case 3 : S=1 , R=0 : Set
o/p Q=1 & $\bar{Q}$=0 & this is Set Condition.

Case 4 : S=1, R=1 : Invalid
Q & $\bar{Q}$ try to become 0 at same time. & this is not acceptable

R-S latch using NAND Gate.

iii) Truth Table :-

S	R	Q	$\bar{Q}$	Remark
0	0	RACE	RACE	RACE
0	1	0	1	Reset
1	0	1	0	Set
1	1	No change	No change	No change

iv) Case 1 : S=0 , R=0 , : RACE
Q & $\bar{Q}$ will be forced to 1. This is undetermined state & hence should be Avoided.

Case 2 : S=0, R=1 : Reset
o/p Q=0 & $\bar{Q}$=1 & this is reset Condition.

Case 3 : S=1 , R=0 : Set
o/p Q=1 & $\bar{Q}$=0 & this is Set Condition.

Case 4 : S=1 , R=1 : No change
There is No change in o/p Condition.

⊛ Triggering Methods :-

i) Triggering is the method → used to determine when a flip-flop or latch responds to it's input signal.

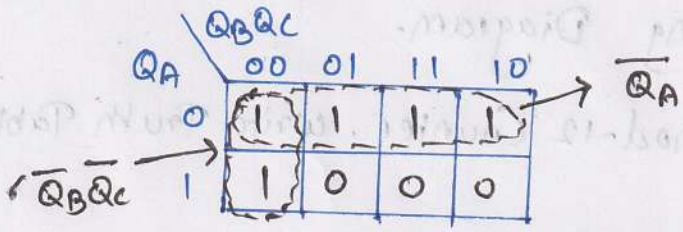
ii) There are Two Types,
   a) Level Triggered circuits
   b) Edge Triggered circuits.

✱ Design a mod-5 ripple Counter using 3-Bit ripple Counter.

⇒ Step 1 :- Truth Table

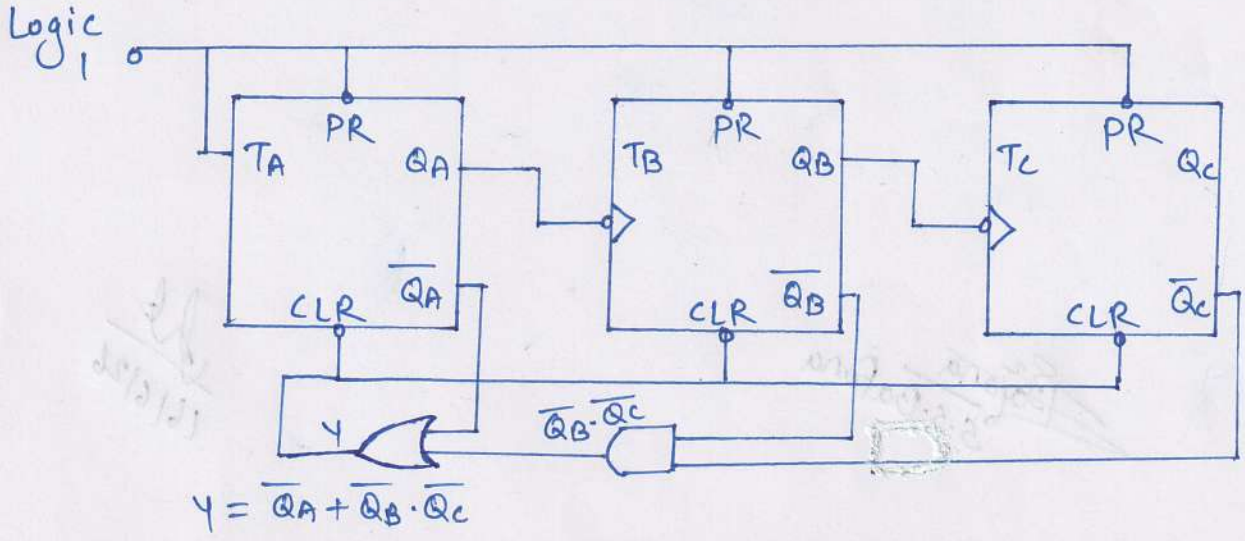
State	flip-flop outputs			Output Y of reset logic	
	Q_A	Q_B	Q_C		
0	0	0	0	1	Valid states
1	0	0	1	1	
2	0	1	0	1	
3	0	1	1	1	
4	1	0	0	1	
5	1	0	1	0	Invalid states
6	1	1	0	0	
7	1	1	1	0	

Step 2 :- k-map



$\therefore Y = \overline{Q_A} + \overline{Q_B}\,\overline{Q_C}$

Step 3 :- Logic Diagram



$Y = \overline{Q_A} + \overline{Q_B} \cdot \overline{Q_C}$

Step 4 :- Timing Diagram.

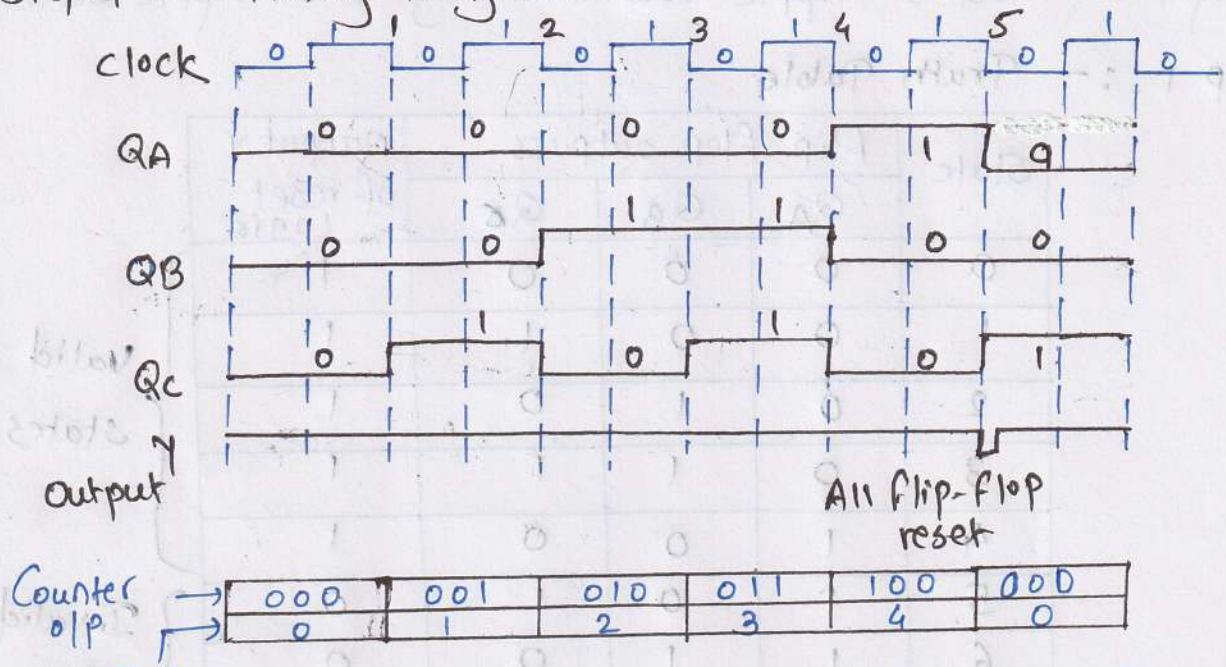


fig. Timing Diagram of mod-5 ripple Counter

Q. Design mod-6 asynchronous Counter. write truth Table and draw timing Diagram.

Q. Design asynchronous mod-12 Counter. write Truth Table and draw waveform.

S. S. Bafana

16/6/26

DIGITAL TECHNIQUES [DTE-313303]

Branch: CO / CW | **QUESTION BANK** | Year: - Second (2nd)

Semester: - Third (3rd) | **Unit 4: Sequential Logic Circuits** | Marks: 18 Marks

Q.1) 02 Marks Question

a) Write truth table for 'D' flipflop & draw its logic diagram using gates. ---(W-25)

b) Write excitation table of T-flip flop ---(S-25)

c) List modes of operation of shift register. ---(W-24)

OR) Name four Types of shift Register. ---(S-24)

d) Differentiate between Latch and flipflop.

Q.2) 04 Marks Question

a) Draw & explain the working of cloked S-R flip flop using NAND gate ---(W-24)

b) what is race-around condition in J-K flipflop ?. How it can be over come and explain the method to over come race around in J-K ---(S-25)

c) Draw & explain 4-bit ring Counter using D-flipflop.

d) Draw logic circuit of J-K flipflop. write it's truth table, excitation table, and one application of J-K flipflop. ---(W-25)

e) Describe working of Serial-in Parallel-out (SIPO) shift register with it's timing diagram. (Use input, "1011" for timing dia.) ---(W-25)

f) what is modulus of Counter ?. Design mod-7 Counter.

g) Explain the working of master slave JK flipflop with truth table and logic diagram. ---(S-23)

Q.3) 06 Marks Questions.

a) Compare Combinational and sequential logic circuit. (Any Six point) ---(S-25)

b) Draw & explain 4-bit twisted ring Counter using J-K flip flop with circuit diagram & Truth Table ---(S-25)

c) Design mod-7 Counter, use k-map and any flipflop, write Truth Table. Draw the timing diagram. ---(W-25)

d) Design mod-10 asynchronous Counter. Draw timing diagram ---(S-25)

e) Draw & explain operation of 4-bit SISO shift register using D flip-flop, with block diagram, truth table and waveform. ---(W-24)

f) Draw 4-bit universal shift register and describe its operation. Also explain the necessity of register in digital circuits. ---(W-23)

9/6/26

Prof. S. S. Bafana