Unit – III Combinational Logic Circuits

Total Marks - 18

Course Title - DIGITAL TECHNIQUES

Course Code - 313303

Programme Name - Computer and Computer Science Engineering

Semester - Third

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Subject - Digital Techniques. (18 marks)

UNIT-3

Combinational Logic Circuits.

Prepared by:- Akshita Jain

3.1 Standard Boolean Expression -

- **Sum of product [SOP] :-**

1) Def^n - SOP is a form of Boolean expression where several product terms (AND operat^n) are added together (OR operat^n)

2) Eg.

$$Y = AB + AC + BC$$

Sum → denotes OR operation

Product of terms → denotes AND operation.

3) Here, A, B, C are the literals or called as inputs of combinational circuits → where as Y is the output.

- **Product of sum [POS] :-**

1) Def^n - POS is a form of Boolean Expression where several Added terms (OR operation) are multiplied together (AND operation).

2) Eg.

$$Y = (A+B) \cdot (B+C) \cdot (A+C)$$

Product (AND operat^n)

Sum of terms (OR operat^n)

3) Here A, B, C are literals or called as inputs of combinational logic circuits, where Y is o/p.

Note - logical expression can be exp in two expression (SOP, POS)

- **Minterm -**

1) **Def^n** - Each individual term → in the canonical SOP (sum of product) form is called minterm.

2) **e.g -**

$$Y = ABC + A\bar{B}\bar{C} + AB\bar{C}$$

↑ ↑ ↑ each individual term is called minterm.

- **Maxterm.**

1) **Def^n** - Each individual term in the canonical POS (Product of sum) form is called maxterm.

2) **e.g.**

$$Y = (A+B) \cdot (\bar{B}+A)$$

↑ ↑ each individual term is called maxterm.

3.2 k-map -

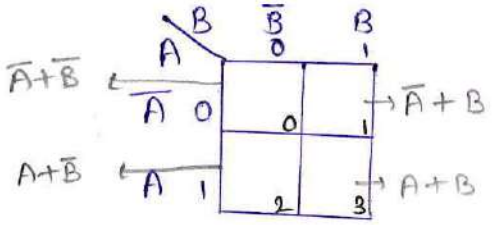
1) k-map stand for "KARNAUGH - MAP"

2) **Def^n** - k-map is the graphical tool → used in Boolean Algebra → It help to reduce the no. of logic gates.

- Rules for k-map simplification -

1) Place 1's in the k-map according to the given minterms.
2) Group must contain 2^n cells (1, 2, 4, 8, ...)
3) Derive the simplified expression from each group.
4) Overlapping is allowed.

1) Two variable k-map - (A, B)

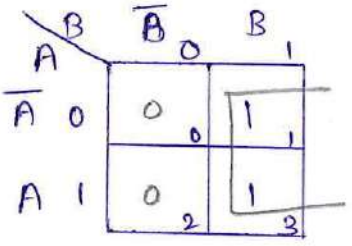


- SOP →
  - 0 → bar (grping)
  - 1 → no bar
- POS →
  - 1 → bar (grping)
  - 0 → no bar.

e.g.

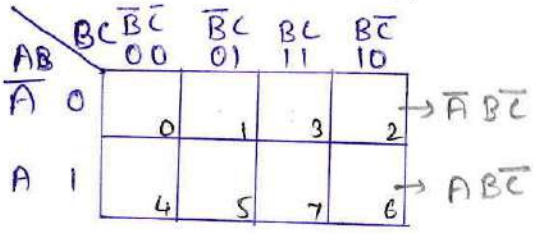
1) $F(A,B) = \Sigma m(1,3)$

→



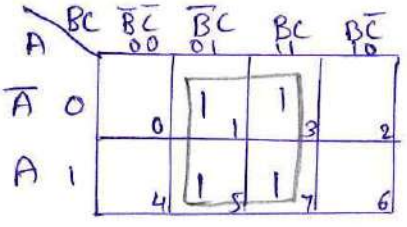
$\boxed{f = B}$

2) Three variable k-map - (A, B, C)



e.g.

1) $f(A,B,C) = \Sigma m(1,3,5,7)$



$\boxed{f = C}$

3) four variable k map. (A, B, C, D)

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0	1	3	2
$\bar{A}B$ 01	4	5	7	6
AB 11	12	13	15	14
$A\bar{B}$ 10	8	9	11	10

eg-

1) $f = (A, B, C, D) = \Sigma m(0, 1, 2, 3)$

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1 (0)	1 (1)	1 (3)	1 (2)
$\bar{A}B$ 01	4	5	7	6
AB 11	12	13	15	14
$A\bar{B}$ 10	8	9	11	10

$$f = \bar{A}\,\bar{B}$$

- Difference between SOP and POS form-

feature	SOP	POS.
full form	Sum of product	Product of sum.
Terms / Structure	AND terms are ORed together	OR terms are ANDed together.
Derived form	Minterms	Maxterms.
grouping	Group 1's	Group 0's.
Standard Notation	Σm (sum of term)	ΠM (Product of term)
Grate Realization	NAND-NAND	NOR-NOR.
Truth table Row used.	Row where o/p = 1	Row where o/p = 0.

• Boolean Expression Reduction using k-map-

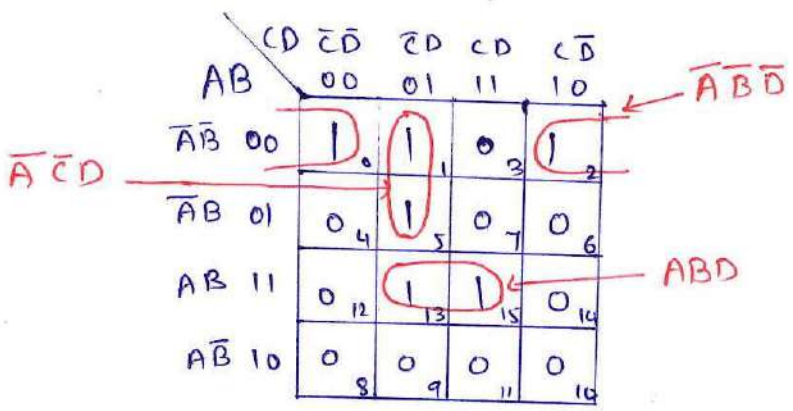
a) Minimizat° of Boolean Expression using Sop form-

• Procedure -

1) Prepared a k-map and place is according to given Truth Table.
2) fill the remaining cells by 0's.
3) Identify the group of 1's [largest grp first] and Prepare an expression for it.
4) Add all the expression together for final output.

Q Logical expression representing a logic circuit is $Y = \Sigma m\ (0,1,2,5,13,15)$. Draw k-map and find the minimized logical expression.

→ We use 4 variable k-map.



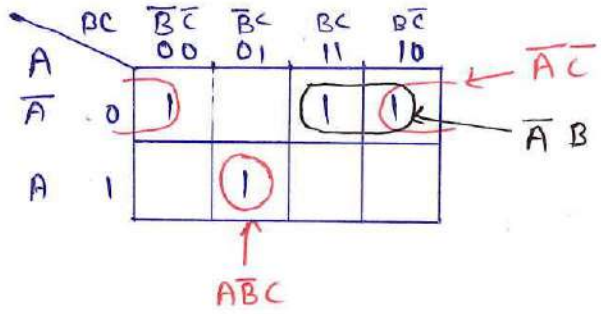
The expression is:-

$$Y = \bar{A}\bar{C}D + \bar{A}\bar{B}\bar{D} + ABD$$

Q. Logical expression in standard SOP form and Draw the logical circuit using logic gates.

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C.$$

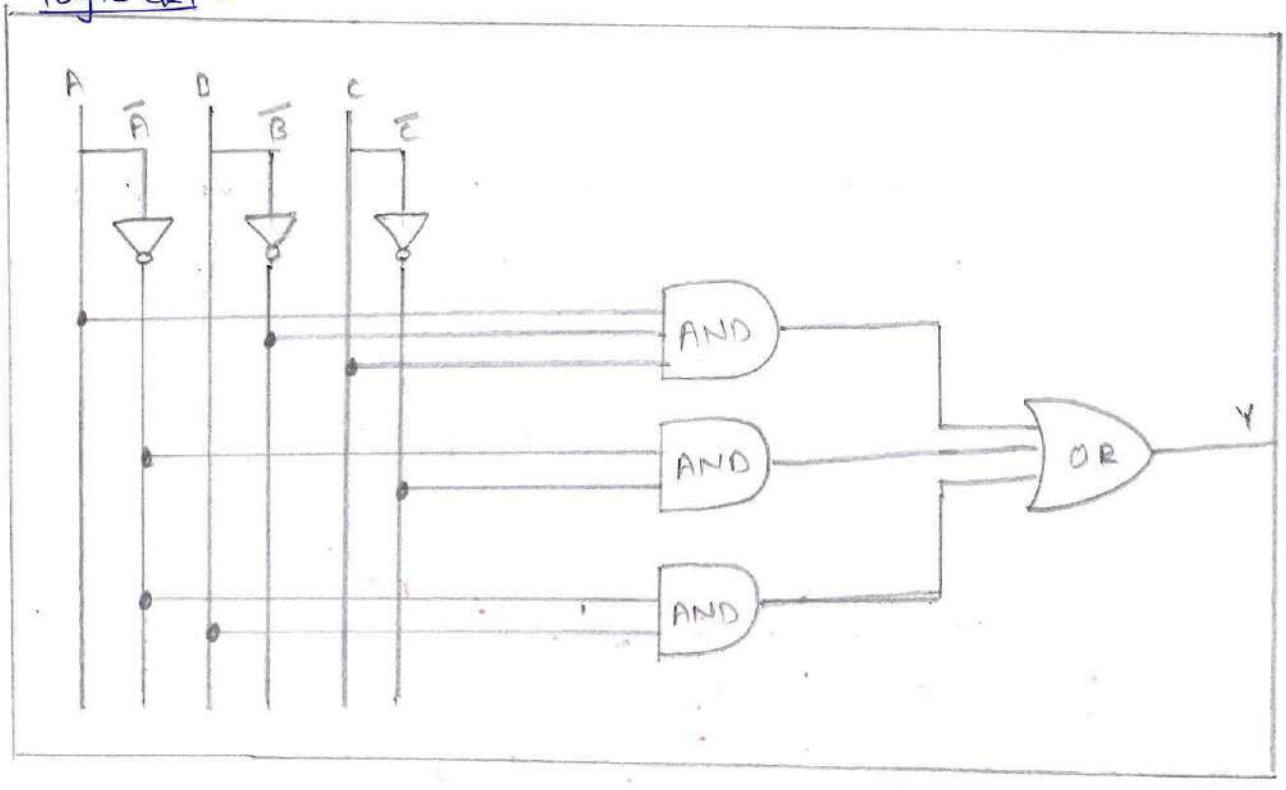
→ We use 3 variable k-map.



final expression is.

$$Y = A\bar{B}C + \bar{A}\bar{C} + \bar{A}B$$

Logic ckt -



b) Minimizat^{n} of Boolean expression using POS form.

- Procedure :-

0 → No bar
1 → bar

1) Prepared a k-map and place is according to given Truth Table.

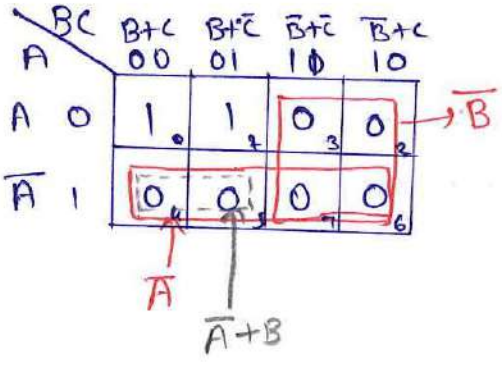
2) fill the remaining cells by 1's.

3) Identify the group of 0's [largest group first] & prepare an expression for it.

4) Add all the expression together for final o/p.

① Solve POS equation using k-map.

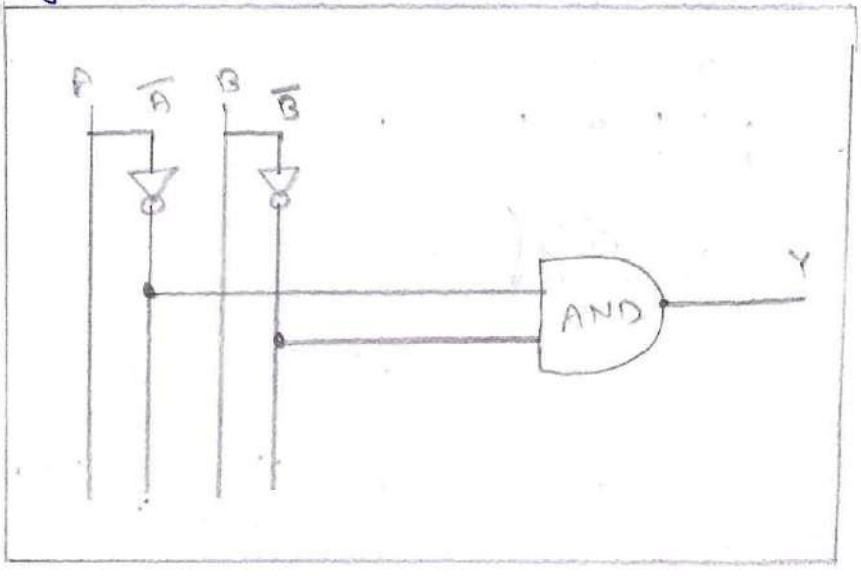
→ $f(A, B, C) = \Pi m(2, 3, 4, 5, 6, 7)$



final expression is,

$$Y = \bar{A} \cdot \bar{B}$$

logical circuit :-



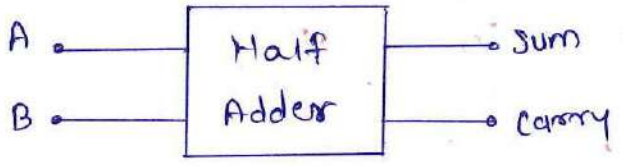
3.3 - Arithemetic circuits-

1) Half Adder
2) full Adder
3) Half Substractor
4) full substractor.

1) Half Adder -

- **Def^n**- Half adder is a combinational logic circuit having two inputs (A, B) and two outputs (sum, carry).

- **Diagram**-

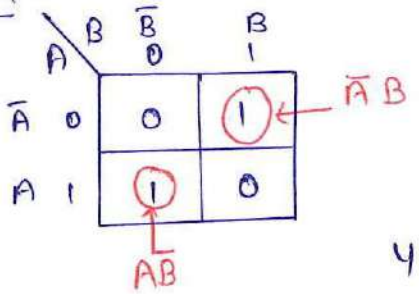


- **Truth Table** -

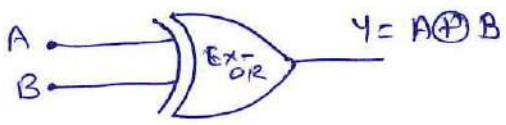
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- **k-map with logic Diagram**-

1) **SUM** -

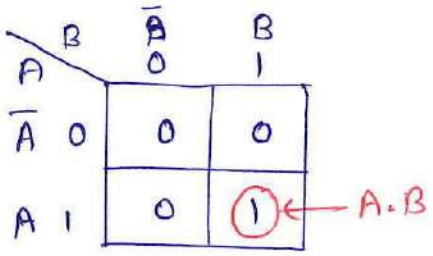


logic Diagram -

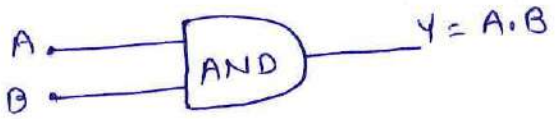


$Y = \bar{A}B + A\bar{B}$ $\therefore$ $\boxed{Y = A \oplus B}$

2) CARRY -



Logic Diagram -

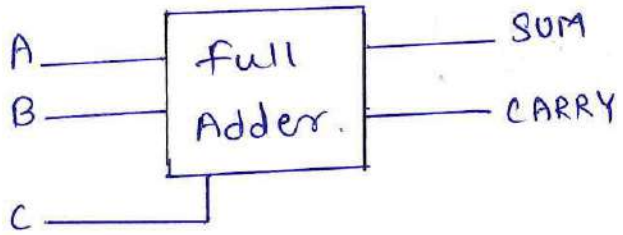


$Y = A.B$

2) Full Adder -

- Def^n - Full adder is a combinational logic circuit having 3 input and two output.

- Diagram -

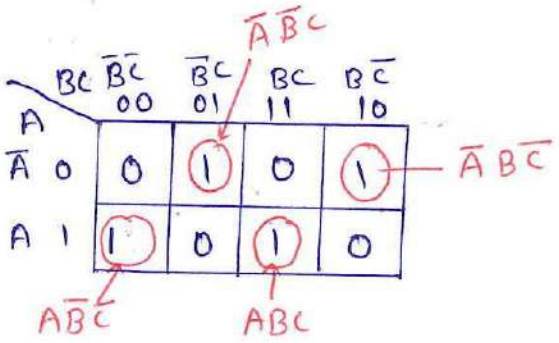


- Truth Table -

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- **k-map with logic Diagram-**

1) **SUM-**



$$Y_S = \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC + \bar{A}B\bar{C}$$

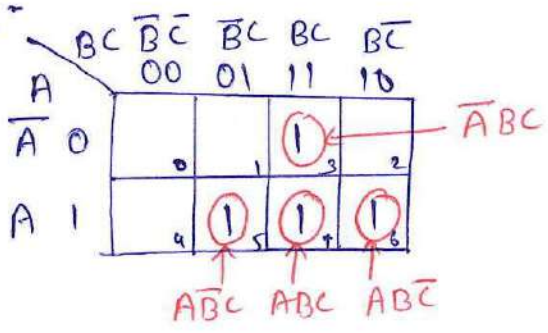
$$= C[\bar{A}\bar{B} + AB] + \bar{C}[\bar{A}B + A\bar{B}] \quad \ldots (A \oplus B)$$

$$= C[\overline{A \oplus B}] + \bar{C}(A \oplus B)$$

$$= C\overline{(A \oplus B)} + \bar{C}(A \oplus B)$$

$$\boxed{Y_S = A \oplus B \oplus C}$$

2) **CARRY-**



$$Y_C = \bar{A}BC + A\bar{B}C + ABC + AB\bar{C}$$

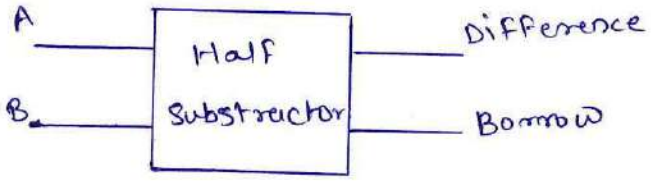
$$= AB(\bar{C} + C) + C(\bar{A}B + A\bar{B}) \quad \ldots (A \oplus B)$$

$$\boxed{Y_C = AB + C(A \oplus B)} \quad \ldots (\bar{C} + C = 1)$$

3) Half Substractor -

- **Def°** - Half Substractor is a combinational logic circuit having two inputs (A, B) and two outputs (Difference, borrow).

- **Diagram** -

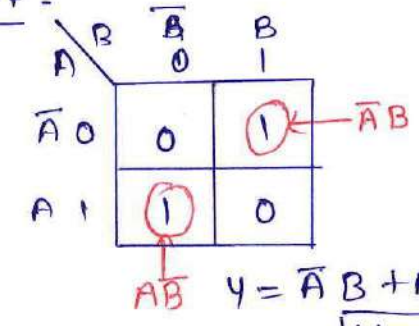


- **Truth Table** -

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

- **k-map with logic Diagram** -

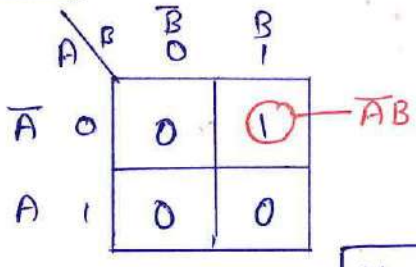
1) **Diff** -



$Y = \bar{A}B + A\bar{B}$

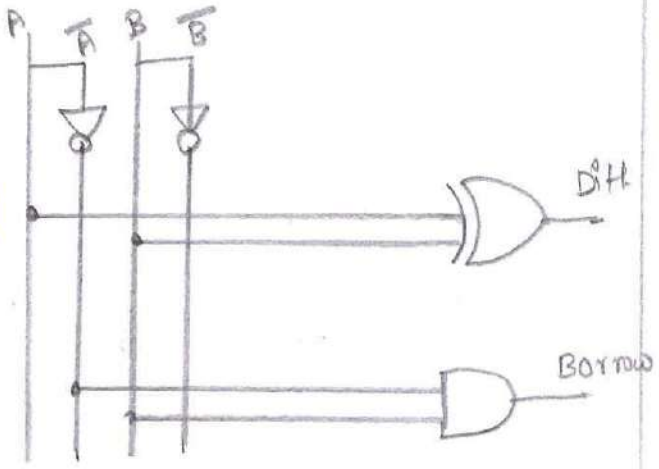
$\boxed{Y = A \oplus B}$

2) **Borrow** -



$\boxed{Y = \bar{A}B}$

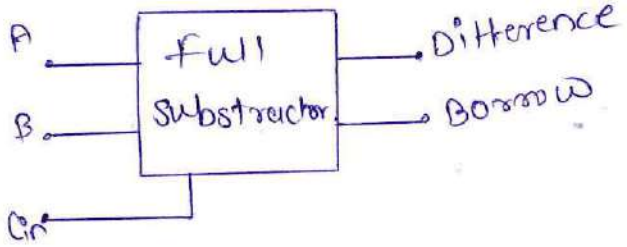
logic Diagram -



4) Full Substractor.

- **Def^n** - full substractor is a combination logic circuit. It having 3 input (A, B, C) and two output (Difference, Borrow).

- **Diagram** -

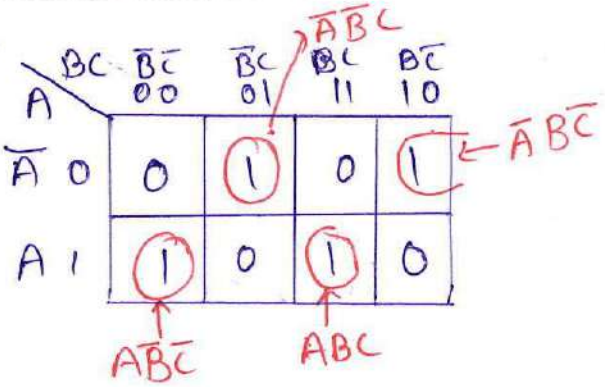


- **Truth Table** -

A	B	C	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

- **k-map with logic Digram :-**

1) **Difference** -



$$Y_D = A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

∴ factoring common terms

$$= C(\bar{A}\bar{B} + AB) + \bar{C}(A\bar{B} + \bar{A}B)$$

∴ Recognizing XOR and XNOR properties.

$$= \bar{A}\bar{B} + AB = A \text{ XNOR } B$$

$$= A\bar{B} + \bar{A}B = A \text{ XOR } B$$

∴ Substitute this value

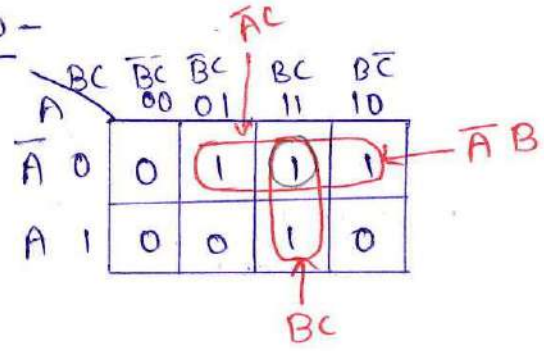
$$= C(A \text{ XNOR } B) + \bar{C}(A \text{ XOR } B)$$

∴ using XNOR Identity

$$Y_D = C \oplus (A \oplus B)$$

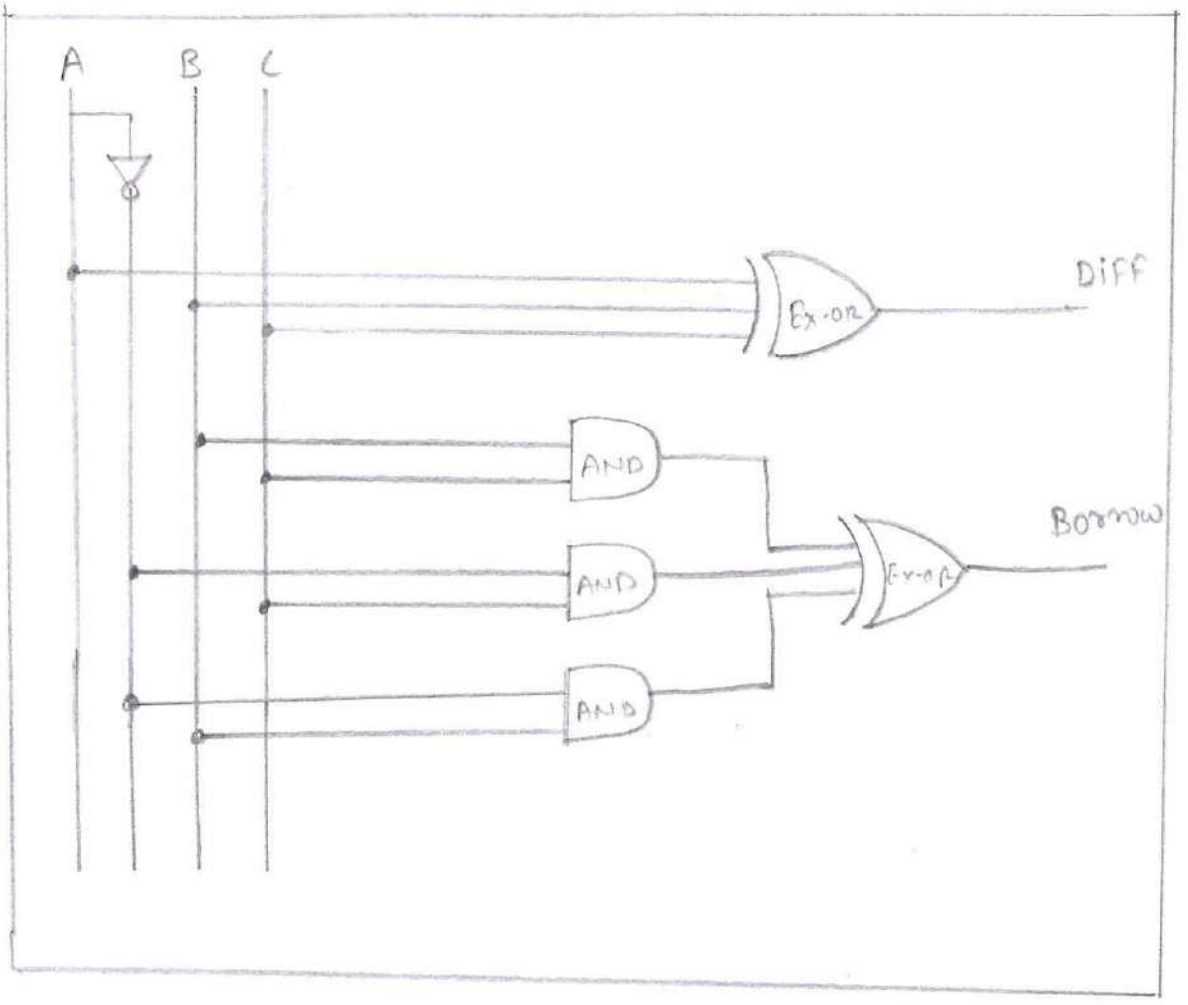
∴ $\boxed{Y_D = C \oplus A \oplus B}$

2) Borrow –



$$Y_B = BC + \bar{A}C + \bar{A}B.$$

Logic Diagram -

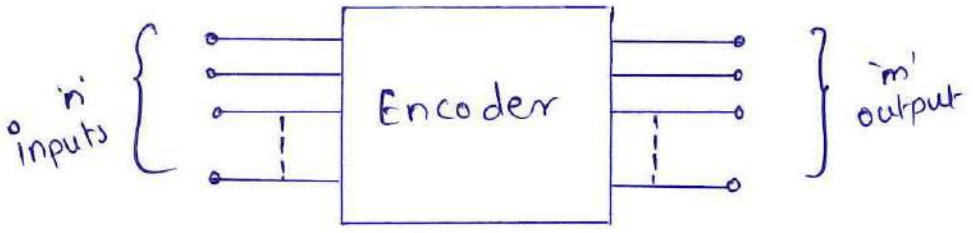


3.4 Encoder and Decoder -

A) Encoder - • Encoder is a combinational logic circuit having 'n' number of input and 'm' number of output to perform inverse operation of decoder.

• Only one input active at a time.

• Diagram -



- **Function of Encoder-**

1) Convert information from Decimal form to binary form.
2) Reduce the no. of transmission line.
3) Used in communication and digital system.

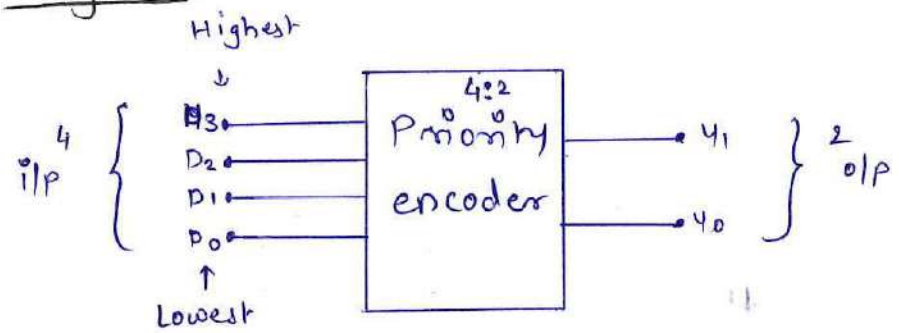
- **Types of Encoder-**

1) Priority encoder (4:2, 8:3)
2) Decimal to BCD encoder.

1) Priority Encoder- (4:2) :-

In A priority encoder is a combinational circuit that outputs the binary code of the highest-priority active input. If multiple inputs are active simultaneously, the input with the highest priority is encoded.

- **Diagram :-**



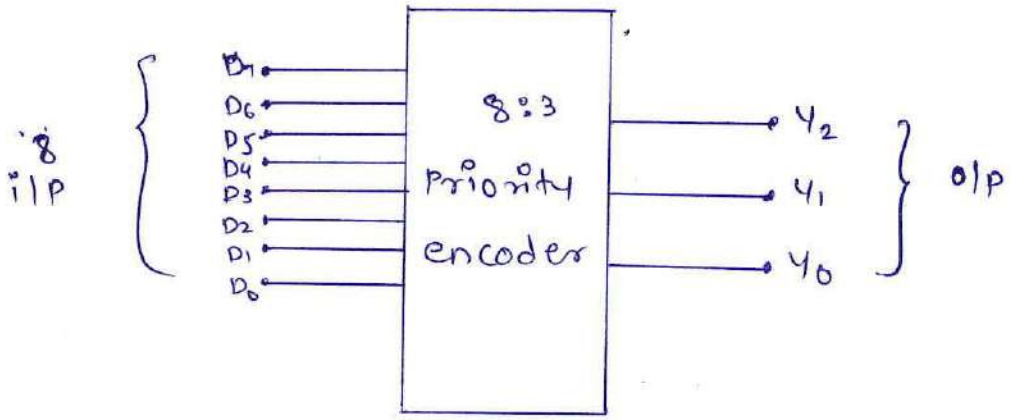
- **Truth Table :-**

Inputs				Outputs	
D_3	D_2	D_1	D_0	Y_1	Y_0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

2) Priority Encoder :- (8:3)

The 8:3 encoder or octal to binary encoder consists of 8 inputs D_7 to D_0 and 3 output (Y_2, Y_1, Y_0).

- **Diagram :-**



- **Truth Table :-**

Inputs								Outputs			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Y_2	Y_1	Y_0	
0	0	0	0	0	0	0	0	x	x	x	
0	0	0	0	0	0	0	1	0	0	0	
0	0	0	0	0	0	1	x	0	0	1	
0	0	0	0	0	1	x	x	0	1	0	
0	0	0	0	1	x	x	x	0	1	1	
0	0	0	1	x	x	x	x	1	0	0	
0	0	1	x	x	x	x	x	1	0	1	
0	1	x	x	x	x	x	x	1	1	0	
1	x	x	x	x	x	x	x	1	1	1	

- **Logica Expression:-**

$$Y_2 = D_7 + D_6 + D_5 + D_4$$

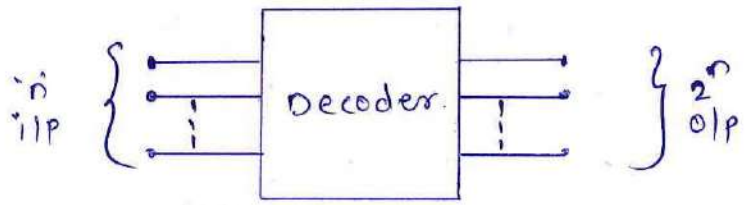
$$Y_1 = D_7 + D_6 + D_3 + D_2$$

$$Y_0 = D_7 + D_5 + D_3 + Y_1.$$

B) Decoder :-

Decoder is a combinational logic circuit having 'n' no. of inputs and '2^n' no. of output Design to perform inverse operation of decoder.

- **Diagram :-**



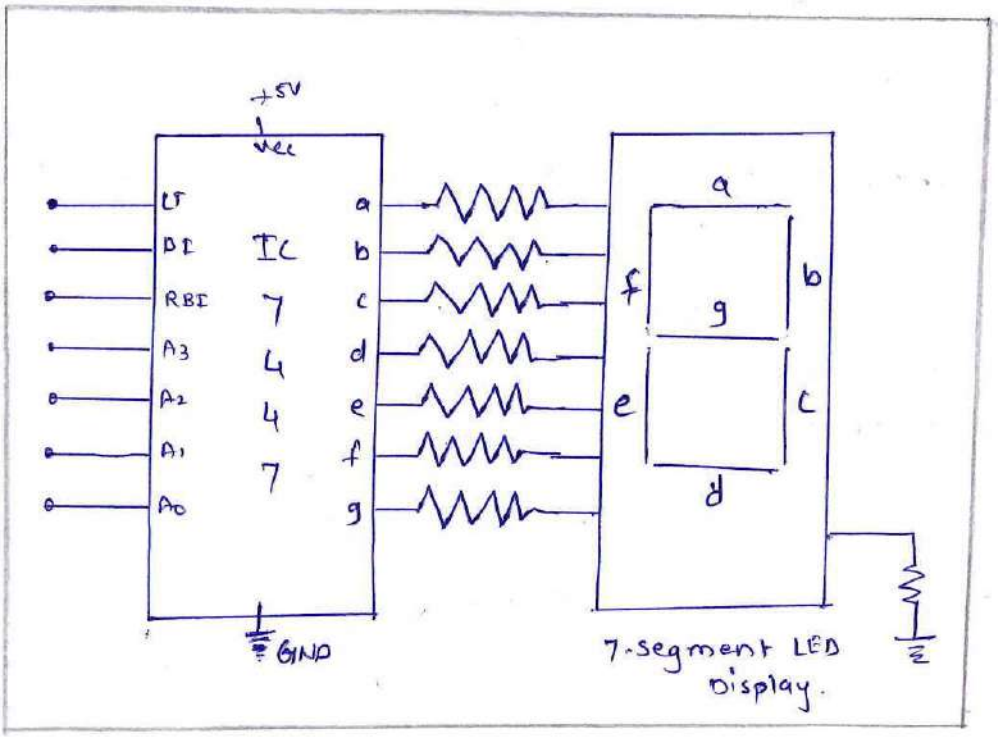
- **function of Encoder :-**

1) Memory address Decoding.
2) Display system.
3) Code Conversion.

- **Types of Decoder :-**

1) BCD to 7 segment Decoder -

1) 7 segment Decoder / Driver Circuit :-



• Truth Table :-

Input	Output						
Decimal	Segments						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

• Keyboard Encoder :-

- keyboard encoder is responsible for converting key presses from a keyboard into digital signal that can be understood by the connected digital system like computer and microcontroller.
- Operation -

keyboard encoder includes following steps -

1. scan matrix
2. key code generation.
3. Interface.
4. output.

1) Scan matrix - The encoder sequencillay scan each row/column to detect is their any key is pressed. in that row/column.

- most keyboard used a matrix of rows and column to identify the key which is pressed.

2) Key code generation - once a key is pressed is detected, the encoder generative a unique key code. corresponding to that key.

3) Interface - keyboard used standard interface to communicate with digital signal.

4) output - The output of keyboard encoder is usually a serial data stream containing the key codes of the pressed keys.
This data stream is transmitted to computered microcontroller for further processing.

- Keyboard Decoder :-

The keyboard decoder on the receiving end interprites the serial data stream. from the encoder and performs necessary action based on key codes received.

- operation -

The operation of keyboard includes :-

1) Data reception - Decoder receives serial data stream containing key codes from the encoder.

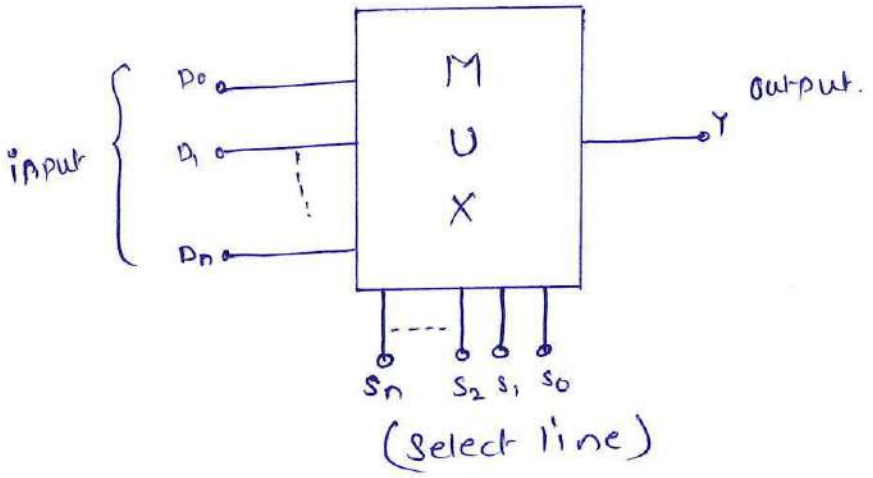
2) key mapping - It maps each received key code to a specific action.

3) Buffering - Decoder includes a buffer to store incomming key codes temporary for smoth functioning even if the system is busy.

3.5 : MULTIPLEXER -

- **Def^n** - Multiplexer is a combinational logic circuit having multiple inputs and only one output along with some select lines.

- **Diagram** -

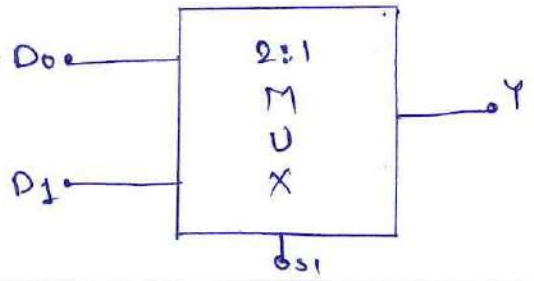


- **List the types of MUX :-**

1) 2:1 MUX
2) 4:1 MUX
3) 8:1 MUX
4) 16:1 MUX
5) 32:1 MUX.

1) **2:1 MUX** - 2:1 MUX is a combinational logic circuit having two inputs and one output along with one select line.

- **Diagram :-**

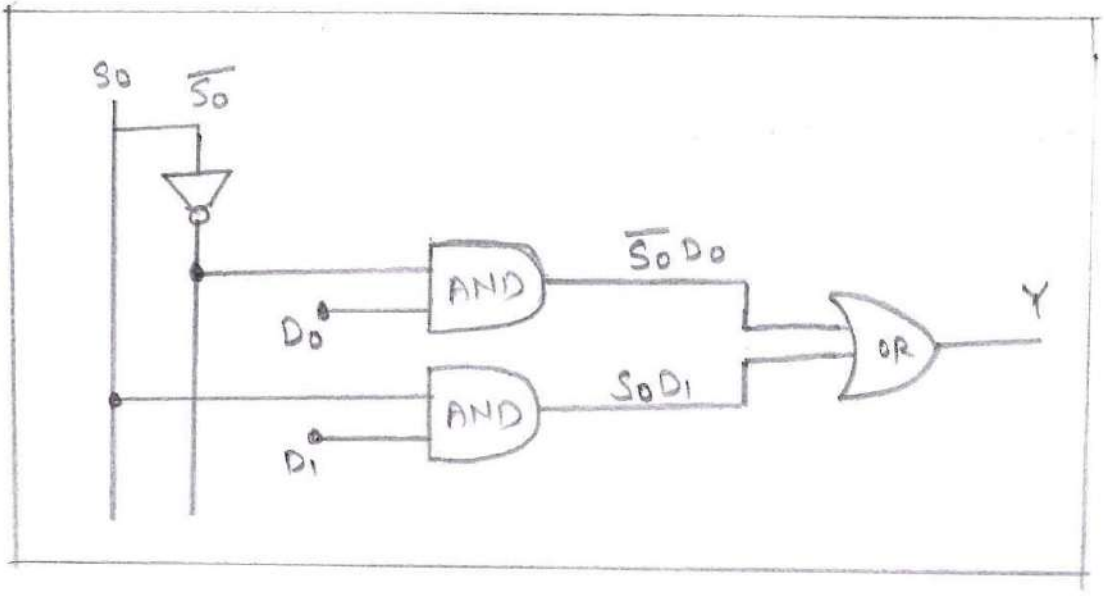


- **Truth Table :-**

S_0	Y	
0	D_0	$\rightarrow \overline{S_0} D_0$
1	D_1	$\rightarrow S_0 D_1$

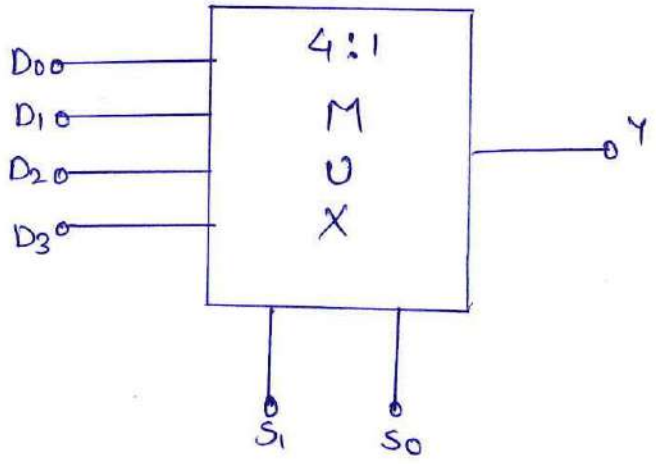
$$Y = \overline{S_0} D_0 + S_0 D_1$$

- **Logic Diagram :-**



2) **4:1 MUX :-** 4:1 mux is a combinational logic circuit having four inputs and one output along with two select lines.

- **Diagram :-**

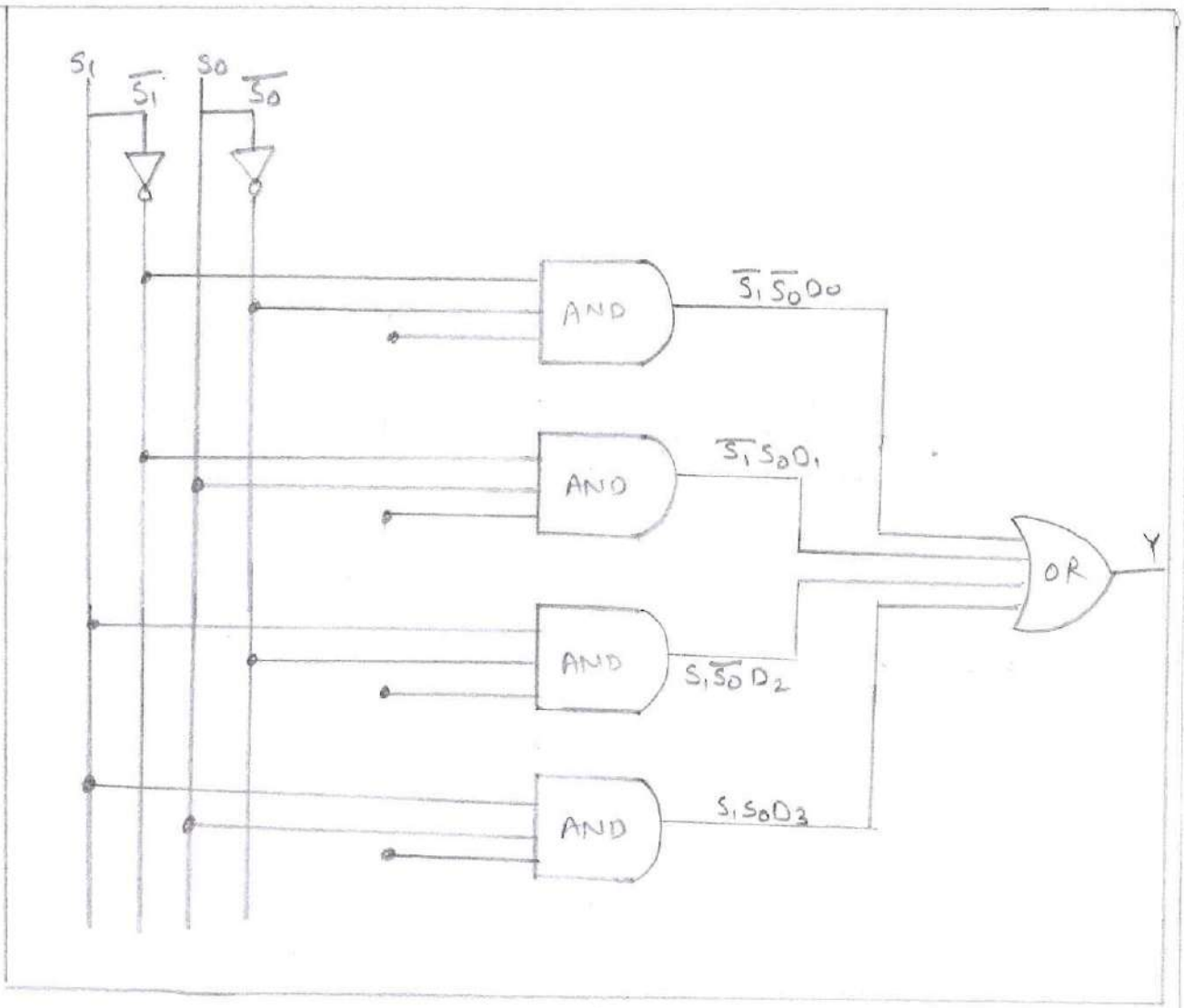


• Truth Table :-

S_1	S_0	Y	
0	0	D_0	$\rightarrow \overline{S_1}\,\overline{S_0} D_0$
0	1	D_1	$\rightarrow \overline{S_1} S_0 D_1$
1	0	D_2	$\rightarrow S_1 \overline{S_0} D_2$
1	1	D_3	$\rightarrow S_1 S_0 D_3$.

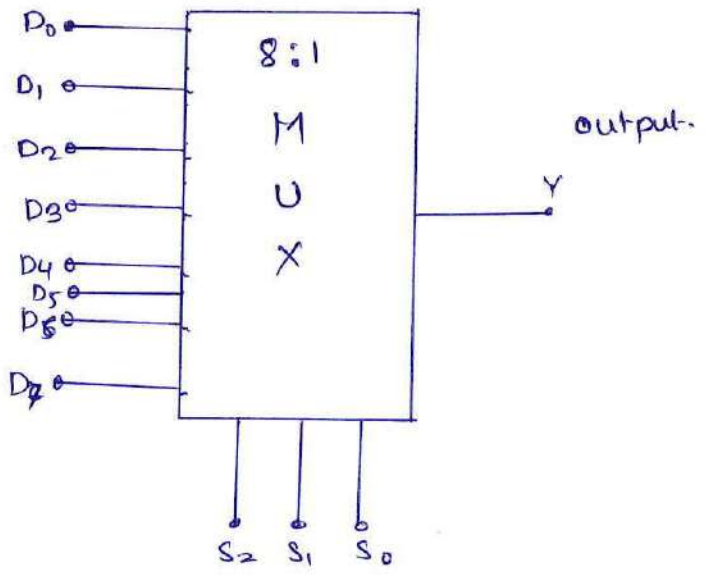
$$Y = \overline{S_1}\,\overline{S_0} D_0 + \overline{S_1} S_0 D_1 + S_1 \overline{S_0} D_2 + S_1 S_0 D_3$$

• Logic Diagram :-



3) 8:1 MUX :- 8:1 mux is a combinational logic circuit having eight inputs and one output along with three select line.

- Diagram :-

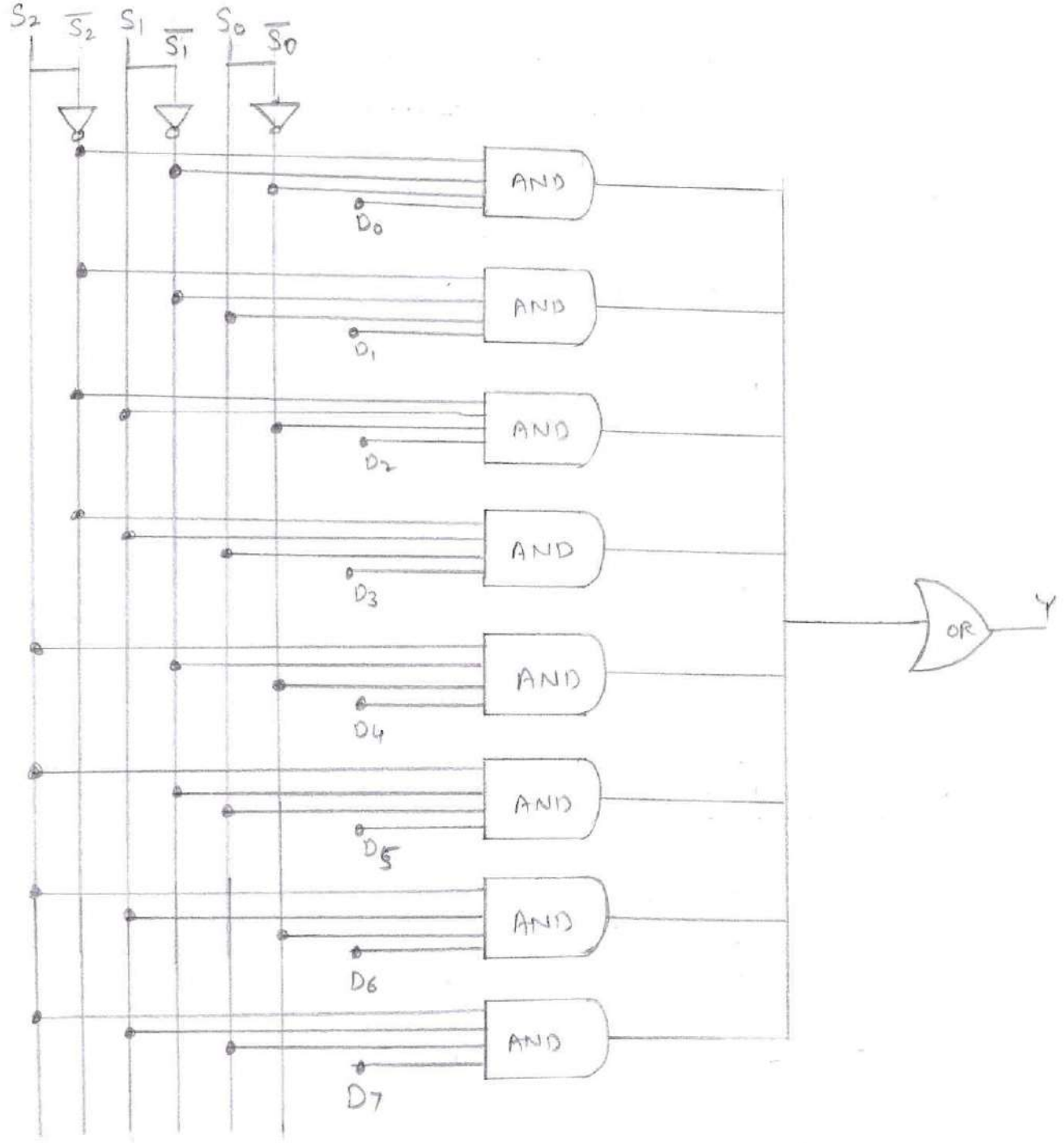


- Truth Table :-

S_2	S_1	S_0	Y	
0	0	0	D0	$\rightarrow \overline{S_2}\,\overline{S_1}\,\overline{S_0}\,D_0$
0	0	1	D1	$\rightarrow \overline{S_2}\,\overline{S_1}\,S_0\,D_1$
0	1	0	D2	$\rightarrow \overline{S_2}\,S_1\,\overline{S_0}\,D_2$
0	1	1	D3	$\rightarrow \overline{S_2}\,S_1\,S_0\,D_3$
1	0	0	D4	$\rightarrow S_2\,\overline{S_1}\,\overline{S_0}\,D_4$
1	0	1	D5	$\rightarrow S_2\,\overline{S_1}\,\overline{S_0}\,D_5$
1	1	0	D6	$\rightarrow S_2\,S_1\,\overline{S_0}\,D_6$
1	1	1	D7	$\rightarrow S_2\,S_1\,S_0\,D_7$

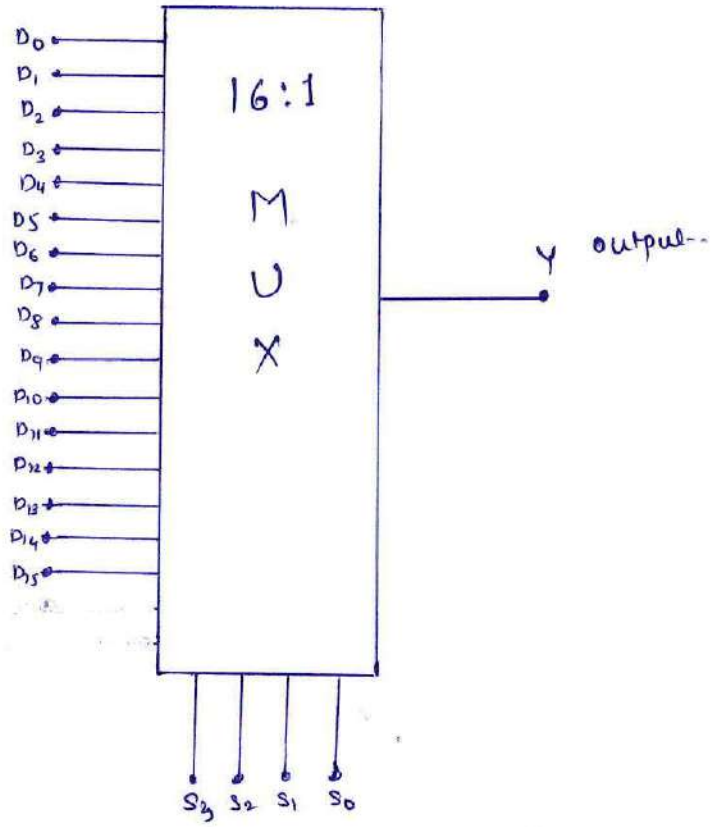
$$Y = \overline{S_2}\,\overline{S_1}\,\overline{S_0}\,D_0 + \overline{S_2}\,\overline{S_1}\,S_0 D_1 + \overline{S_2}\,S_1\,\overline{S_0}\,D_2 + \overline{S_2}\,S_1\,S_0 D_3 + S_2\,\overline{S_1}\,\overline{S_0}\,D_4 + S_2\,\overline{S_1}\,\overline{S_0}\,D_5 + S_2\,S_1\,\overline{S_0}\,D_6 + S_2\,S_1\,S_0 D_7.$$

• Logic Diagram :-



4) 16:1 MUX :- 16:1 MUX is combinational logic circuit having 16 inputs and one output along with four select line.

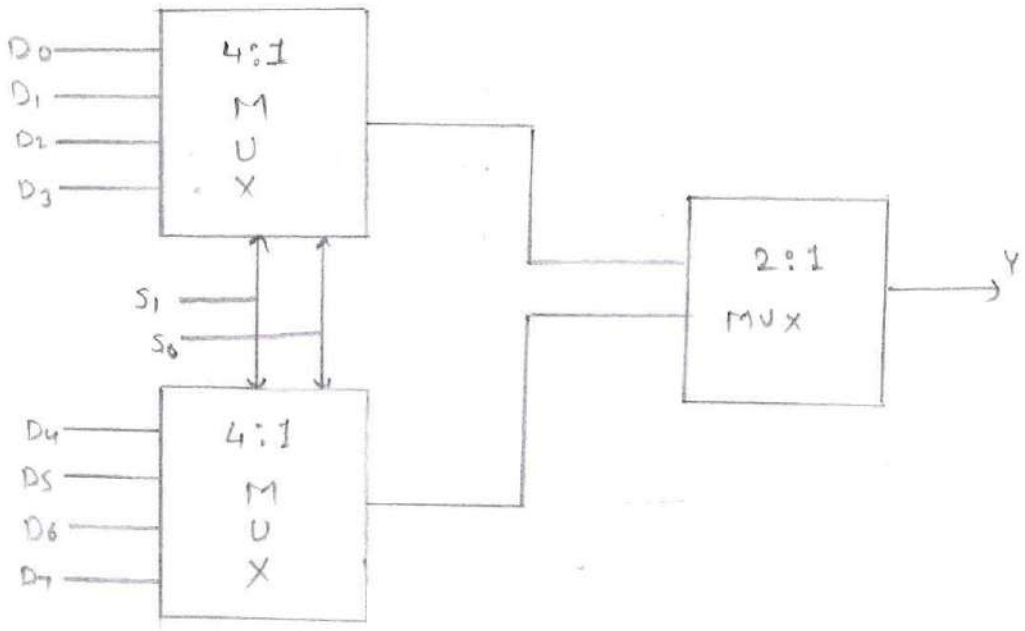
• Diagram :-



• Truth Table :-

S_3	S_2	S_1	S_0	Y	
0	0	0	0	D_0	$\rightarrow \overline{S_3}\,\overline{S_2}\,\overline{S_1}\,\overline{S_0}\,D_0$
0	0	0	1	D_1	$\rightarrow \overline{S_3}\,\overline{S_2}\,\overline{S_1}\,S_0\,D_1$
0	0	1	0	D_2	$\rightarrow \overline{S_3}\,\overline{S_2}\,S_1\,\overline{S_0}\,D_2$
0	0	1	1	D_3	$\rightarrow \overline{S_3}\,\overline{S_2}\,S_1\,S_0\,D_3$
0	1	0	0	D_4	$\rightarrow \overline{S_3}\,S_2\,\overline{S_1}\,\overline{S_0}\,D_4$
0	1	0	1	D_5	$\rightarrow \overline{S_3}\,S_2\,\overline{S_1}\,S_0\,D_5$
0	1	1	0	D_6	$\rightarrow \overline{S_3}\,S_2\,S_1\,\overline{S_0}\,D_6$
0	1	1	1	D_7	$\rightarrow \overline{S_3}\,S_2\,S_1\,S_0\,D_7$
1	0	0	0	D_8	$\rightarrow S_3\,\overline{S_2}\,\overline{S_1}\,\overline{S_0}\,D_8$
1	0	0	1	D_9	$\rightarrow S_3\,\overline{S_2}\,\overline{S_1}\,S_0\,D_9$
1	0	1	0	D_{10}	$\rightarrow S_3\,\overline{S_2}\,S_1\,\overline{S_0}\,D_{10}$
1	0	1	1	D_{11}	$\rightarrow S_3\,\overline{S_2}\,S_1\,S_0\,D_{11}$
1	1	0	0	D_{12}	$\rightarrow S_3\,S_2\,\overline{S_1}\,\overline{S_0}\,D_{12}$
1	1	0	1	D_{13}	$\rightarrow S_3\,S_2\,\overline{S_1}\,S_0\,D_{13}$
1	1	1	0	D_{14}	$\rightarrow S_3\,S_2\,S_1\,\overline{S_0}\,D_{14}$
1	1	1	1	D_5	$\rightarrow S_3\,S_2\,S_1\,S_0\,D_{15}$.

Q1. Implement 8:1 MUX using 4:1 MUX.



Q2. Design 16:1 Multiplexer using 8:1 Multiplexer.

→ Input - 16
Output - 01
Select line - 04
8:1 Mux - 02
2:1 mux - 01

Q3. Design 16:1 Multiplexer using 4:1 multiplexer.

→ Input - 16
Output - 01
Select line - 04
4:1 mux - 5

Q4. Design 4:1 ~~mux~~ multiplexer using 2:1 multipler.

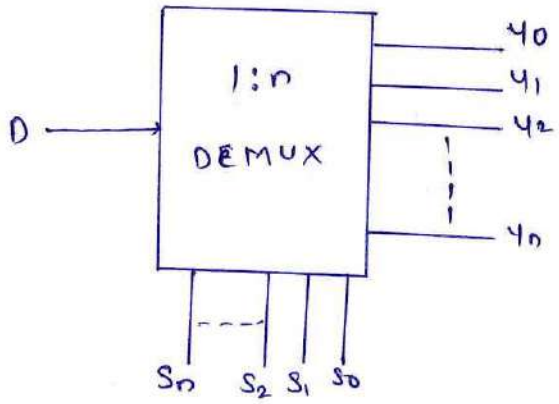
→ Input - 4
Output - 01
select line - 2
2:1 Mux - 3

(Note:- Student have to draw Appropriate Diagram for ~~Q~~ que 2, 3, 4.)

3.6 - DEMULTIPLEXER -

- **Def^n** - Demultiplexer is a combinational logic circuit having only one input and multiple output with some select line.

- **Diagram** -

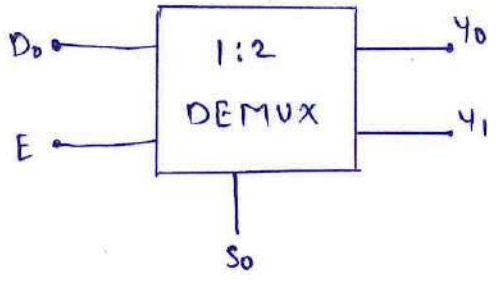


- **List Types of DEMUX :-**

1) 1:2 DEMUX
2) 1:4 DEMUX
3) 1:8 DEMUX
4) 1:16 DEMUX
5) 1:32 DEMUX.

1) 1:2 DEMUX :- 1:2 DEMUX is a combinational logic circuit having one input and two output along with one select line.

- **Diagram :-**

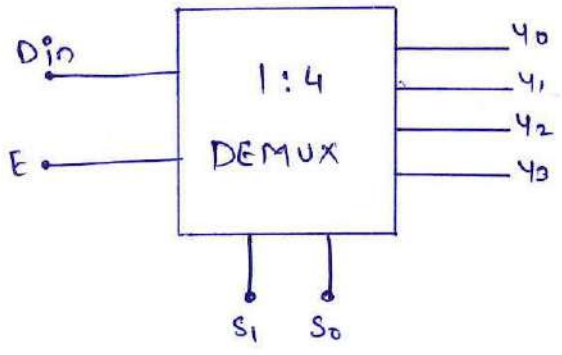


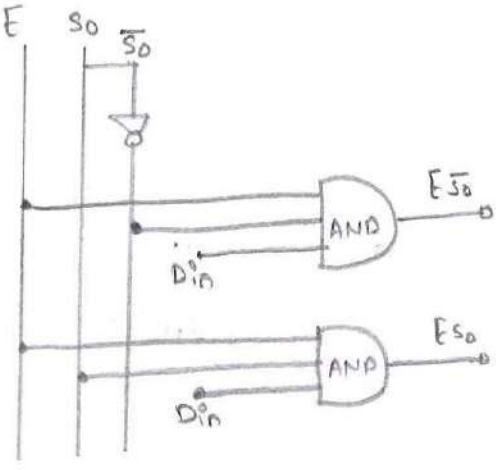
• Truth Table :-

Input		output.		
E	S_0	Y_0	Y_1	
0	x	0	0	
1	0	Din	0	$\rightarrow E\bar{S_0}Din$
1	1	0	Din	$\rightarrow E S_0 Din$.

2) 1:4 DEMUX :- 1:4 DEMUX is a combinational logic circuit having one input and four o/p along with two select line.

• Diagram :-

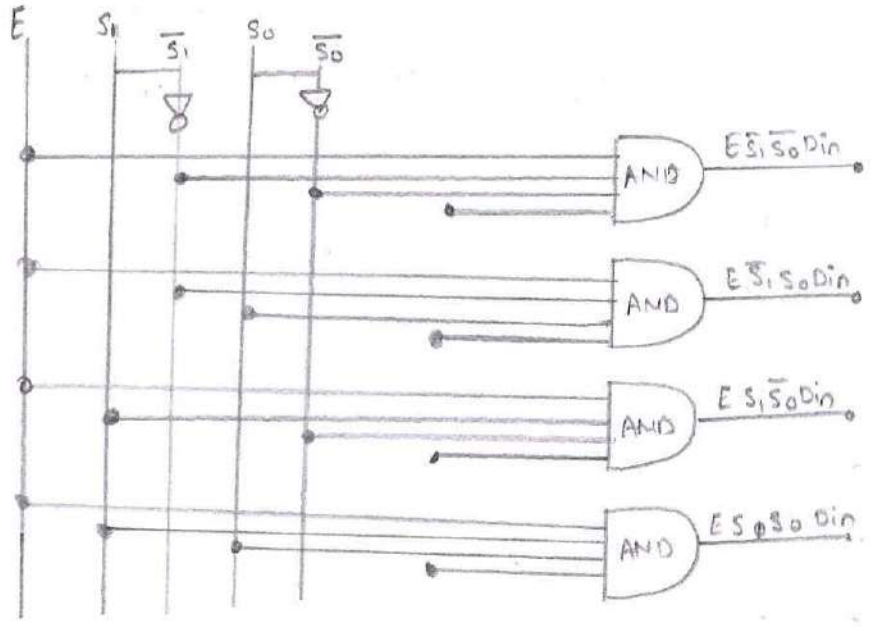




• Truth Table :-

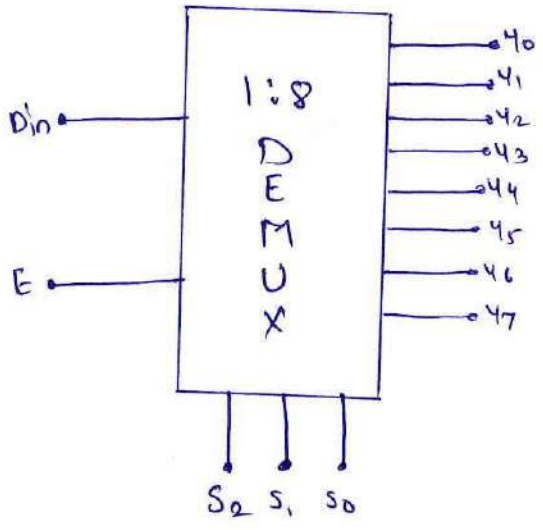
Input			output.				
E	S_1	S_0	Y_0	Y_1	Y_2	Y_3	
0	x	Y	0	0	0	0	$\rightarrow$
1	0	0	Din	0	0	0	$\rightarrow E\bar{S_1}\bar{S_0}Din$
1	0	1	0	Din	0	0	$\rightarrow E\bar{S_1}S_0Din$
1	1	0	0	0	Din	0	$\rightarrow S_1\bar{S_0}Din$
1	1	1	0	0	0	Din	$\rightarrow S_1S_0Din$

• Logic Diagram :-



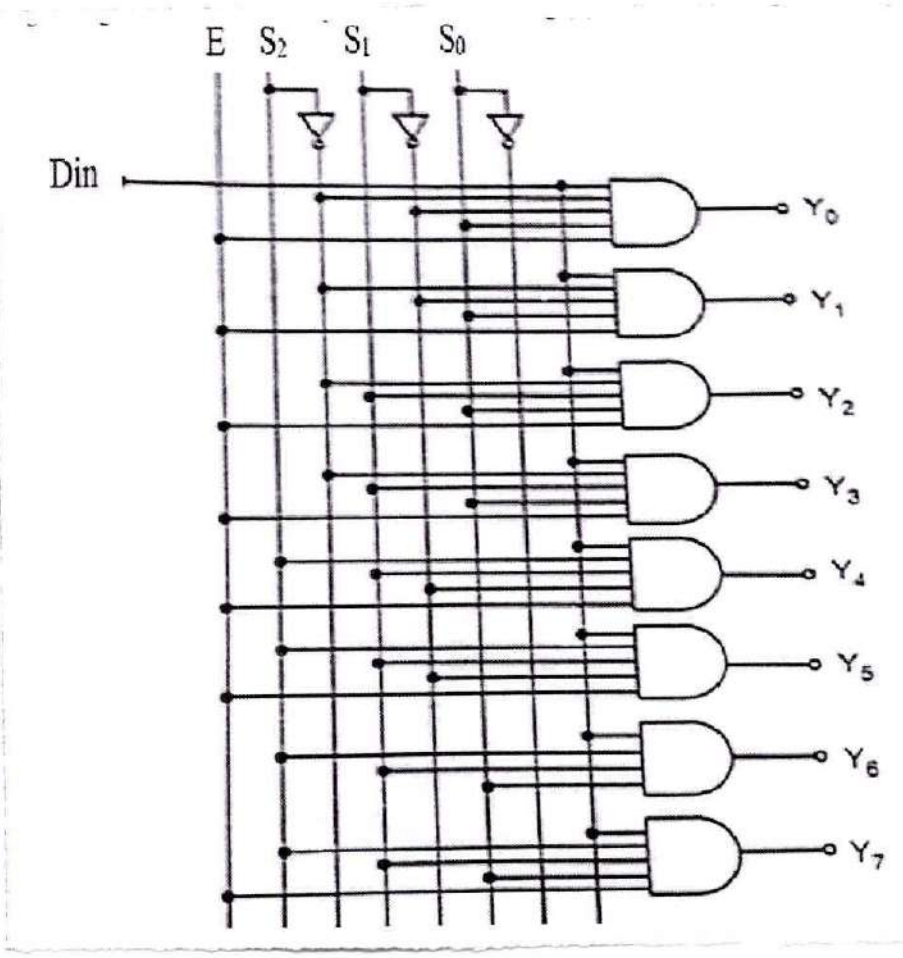
3) 1 : 8 DEMUX :- 1:8 DEMUX is a combinational logic circuit having one input and eight outputs along with three select lines.

• Diagram :-

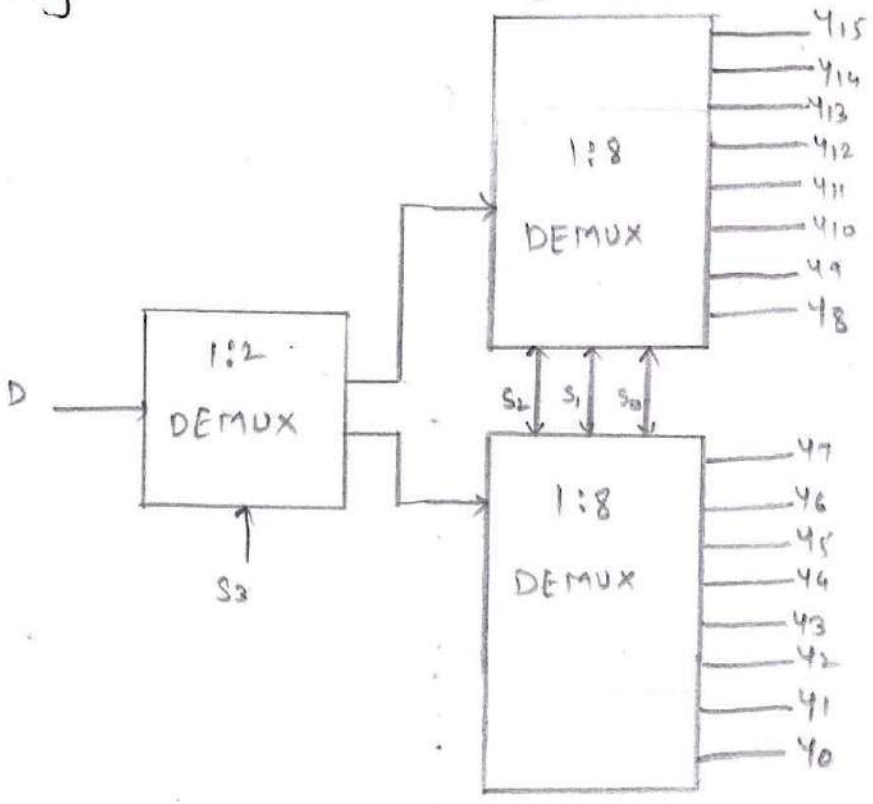


• Truth Table :-

Input				output.							
E	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	Din	0	0	0	0	0	0	0
1	0	0	1	0	Din	0	0	0	0	0	0
1	0	1	0	0	0	Din	0	0	0	0	0
1	0	1	1	0	0	0	Din	0	0	0	0
1	1	0	0	0	0	0	0	Din	0	0	0
1	1	0	1	0	0	0	0	0	Din	0	0
1	1	1	0	0	0	0	0	0	0	Din	0
1	1	1	1	0	0	0	0	0	0	0	Din



Q. Design 1:16 DEMUX using 1:8 DEMUX.



- **Application of Multiplexer :-**

1) Data Routing
2) Communication System.
3) Telephone network.
4) Logic function Generation.

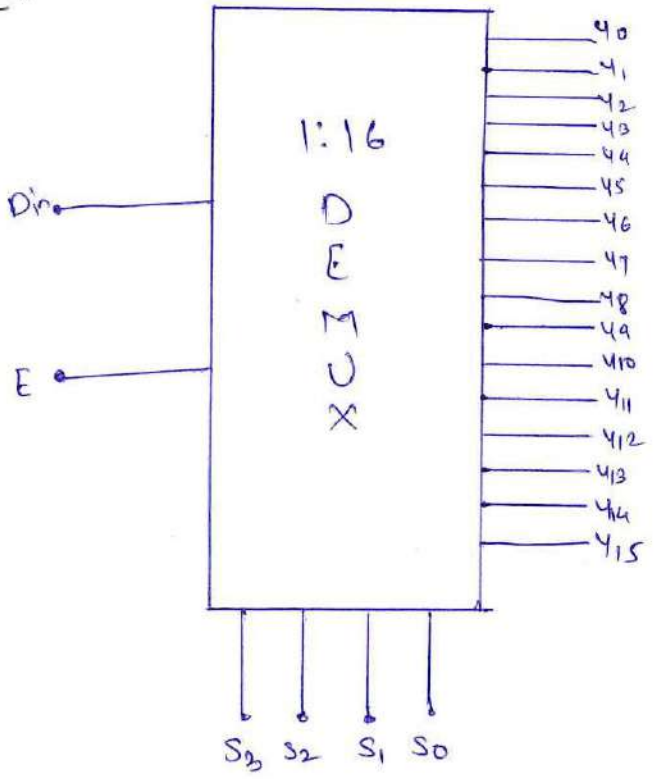
- **Application of Demultiplexer :-**

1) Data Distribution.
2) Control signal Distribution.
3) Computer network.
4) Memory Address Decoding.

4) 1:16 DEMUX :-

- **Def^n** - 1:16 DEMUX is a combinational logic circuit having one output and 16 input ~~and~~ along with 4 select lines.

- **Diagram :-**



- **Truth table :-**

Enable	Select inputs				outputs															
E	S_3	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	D_{in}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	D_{in}	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	D_{in}	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	D_{in}	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	D_{in}	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	D_{in}	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	D_{in}	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	D_{in}	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	D_{in}	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	D_{in}	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D_{in}	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	D_{in}	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D_{in}	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D_{in}	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D_{in}	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D_{in}

@ksdas

8/6/16

Unit 3
Combinational Logic circuits

QUESTION BANK

1) Define and Draw logic symbol of Demultiplexeer. (2 marks)
2) Implement full Adder using two Half Adder (4 marks)
3) Design 32:1 multiplexer using 8:1 multiplexeer. (4 marks)
4) Minimize the following equation using k-map.
$Y = \Sigma m\ (0,2,5,7,8,10,13,15)$
Realize the minimized expression using logic gates. (6 marks)
5) Draw full substractor circuits logic diagram, truth table and k-map simplification. (4 mark)
6) Design 16:1 multiplexer using 4:1 multiplexer. (4 marks)
7) Draw the logical circuit diagram of BCD of 7 segment decoder & write its truth table. (4 marks)
8) Define SOP form and POS form of Boolean expression Convert $f(A,B,C) = \Sigma m(1,4,5,6,7)$ in Standard POS form. (6 marks)
9) Compare Combinational & sequential logic ckt. (4/6 marks)
10) Draw the block Diagram of 8:3 priority encoder with truth table. (4 marks)
11) State any two Application of MUX and DEMUX (4 marks)
12) State any two Application of Encoder and Decoder (4 marks)
13) Derive the expression for sum and carry using k-map.
14) Explain Minterm and Maxterm (4 marks)
15) Minimize following fun° & realize it using minimun no. of logic gate (use k-map) i) $f = \Pi m\ (2,7,10,11,12,15)$

16) Design half Adder using k-map and logic gates. (4marks)

17) Design half substractor using k-map. (4 marks)

18) Draw the block Diagram and truth table of a 4:2 Encoder. (4marks)

19) Draw 1:8 demux using 1:2 demultiplexer. (4marks)

20) Realize a Boolean function using only NAND gates and NOR gates . (6 marks).

$$f = \overline{A}\,\overline{B} + AB.$$

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6/6/26

6-6-26.